Marconi
Instruments

Please keep this

INSTRUCTION BOOK

with the equipment

TYPE No. 52022-900

119021

MARCONI INSTRUMENTS LIMITED
ST. ALBANS HERTFORDSHIRE ENGLAND

10 kHz - 1000.000 MHz

AM/FM SIGNAL GENERATOR
2022

Code No. 52022-900C

AMENDMENT RECORD

The following amendments are incorporated in this manual.

Amendment No.	Date	Issued at Serial number
Commencing	July 84	119001
Am. 1	Apr. 85	119004/001
Am. 2	Sep. 86	119027/035

Part No. 46881-515U
Print code: C-9/86 MI 1.03c

CONTENTS

HAZARD WARNING SYMBOLS

The following symbols appear on the equipment

Symbol	Type of hazard	Reference in manual
⚠	Static sensitive device	Page (iv)

Note ...

Each page bears the data of the original issue or the code number and date of the latest amendment (Am. 1, Am. 2 etc.). New or amended material of technical importance introduced by the latest amendment is indicated by triangles positioned thus ▶.....◀ to show the extent of the change. When a chapter is reissued the triangles do not appear. Any changes subsequent to the latest amendment state of the manual are included on inserted sheets coded C1, C2 etc.

SECURITY NOTICE

Second functions are grouped into three levels of operation. Access to the first two groups, Normal and First level operation can be freely gained by carrying out the unlocking procedures described in both Operating manual and Service manual. Details for accessing the Second level operation however are only included in the Service manual. Some user units may wish to further restrict the distribution of this information to selected calibration areas only. To enable this, alternative Chapter 4, pages 41a/42a have been included which have the unlocking procedure deleted. Users may then withdraw either pages 41/42 or 41a/42a as required.

NOTES AND CAUTIONS

ELECTRICAL SAFETY PRECAUTIONS

This equipment is protected in accordance with IEC Safety Class 1. It has been designed and tested according to IEC Publication 348, "Safety Requirements for Electronic Measuring Apparatus", and has been supplied in a safe condition. The following precautions must be observed by the user to ensure safe operation and to retain the equipment in a safe condition.

Defects and abnormal stresses

Whenever it is likely that protection has been impaired, for example as a result of damage caused by severe conditions of transport or storage, the equipment shall be made inoperative and be secured against any unintended operation.

Removal of covers

Removal of the covers is likely to expose live parts although reasonable precautions have been taken in the design of the equipment to shield such parts. The equipment shall be disconnected from the supply before carrying out any adjustment, replacement, or maintenance and repair during which the equipment shall be opened. If any adjustment, maintenance or repair under voltage is inevitable it shall only be carried out by a skilled person who is aware of the hazard involved.

Note that capacitors inside the equipment may still be charged when the equipment has been disconnected from the supply. Before carrying out any work inside the equipment, capacitors connected to high voltage points should be discharged; to discharge mains filter capacitors, if fitted, short together the L (live) and N (neutral) pins of the mains plug.

Mains plug

The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action shall not be negated by the use of an extension lead without protective conductor. Any interruption of the protective conductor inside or outside the equipment is likely to make the equipment dangerous.

Fuses

Note that there is a supply fuse in both the live and neutral wires of the supply lead. If only one of these fuses should rupture, certain parts of the equipment could remain at supply potential.

To provide protection against breakdown of the supply lead, its connectors, and filter where fitted, an external supply fuse (e.g. fitted in the connecting plug) should be used in the live lead. The fuse should have a continuous rating not exceeding 6 A.

Make sure that only fuses with the required rated current and of the specified type are used for replacement. The use of mended fuses and the short-circuiting of fuse holders shall be avoided.

RADIO FREQUENCY INTERFERENCE

This equipment conforms with the requirements of IEC Directive 76/889 as to limits of r.f. interference.

CAUTION : STATIC SENSITIVE COMPONENTS

Components identified with the symbol ⚠ on the circuit diagrams and/or parts lists are static sensitive devices. The presence of such devices is also indicated in the equipment by orange discs, flags or labels bearing the same symbol. Certain handling precautions must be observed to prevent these components being permanently damaged by static charges or fast surges.

(1) If a printed board containing static sensitive components (as indicated by a warning disc or flag) is removed, it must be temporarily stored in a conductive plastic bag.

(2) If a static sensitive component is to be removed or replaced the following anti-static equipment must be used.

A work bench with an earthed conductive surface.

Metallic tools earthed either permanently or by repeated discharges.

A low-voltage earthed soldering iron.

An earthed wrist strap and a conductive earthed seat cover for the operator, whose outer clothing must not be of man-made fibre.

(3) As a general precaution, avoid touching the leads of a static sensitive component. When handling a new one, leave it in its conducting mount until it is required for use.

(4) If using a freezer aerosol in fault finding, take care not to spray programmable ICs as this may affect their contents.

CAUTION : LCD HANDLING

When operating or servicing this equipment take care not to depress the front or rear faces of the display module as this may damage the liquid crystal display elements.

WARNING : HANDLING HAZARDS

This equipment is formed from metal pressings and although every endeavour has been made to remove sharp points and edges care should be taken, particularly when servicing the equipment, to avoid minor cuts.

WARNING : TOXIC HAZARD

Many of the electronic components used in this equipment employ resins and other chemicals which give off toxic fumes on incineration. Appropriate precautions should therefore be taken in the disposal of these items.

Chapter 4

TECHNICAL DESCRIPTION

CONTENTS

CONTENTS (continued)

INTRODUCTION

1. The following summary is an outline description of the instrument which may be read in conjunction with two simplified block diagrams. The first is found in the Operating Manual and provides a simple guide to the main method of signal frequency generation in the instrument. A more detailed diagram giving more specific information can be found in Chap. 7, Fig. 1 of the Service Manual.

OVERALL TECHNICAL DESCRIPTION

Frequency synthesizer and signal processing

2. 2022 is a synthesized a.m., f.m. or phase modulated signal generator covering a frequency range of 10 kHz - 1000 MHz. Frequencies in the range 250 - 500 MHz are generated from two voltage controlled oscillators. In the range 62.5 to 250 MHz signal frequencies are obtained by divider circuits and in the range 10 kHz to 62.5 MHz, by a beat frequency oscillator (b.f.o.) system. A frequency doubler is used to cover the band 500 - 1000 MHz.

3. The output frequency is phase locked to a frequency standard and frequencies up to 100 MHz can be set to a resolution of 10 Hz. Above 100 MHz the resolution is 100 Hz. A fractional division scheme allows this resolution to be obtained whilst still keeping the phase locked loop (p.l.l.) bandwidth

reasonably high. Provision is also made for the use of an external frequency standard when this is preferred. Frequencies of 10, 5 or 1 MHz can be used depending on the position of an internal link fitted within the instrument.

Output

4. Calibrated output levels from -127 dBm to +6 dBm in the c.w. and f.m. modes and up to 0 dBm in the a.m. mode are provided. A combination of ten output level calibration units can be selected on the front panel. The r.f. output level can be set to a resolution of 0.1 dB over the entire output voltage range and features a total cumulative accuracy of ±2 dB. A precision attenuator provides 120 dB in 10 dB steps and is a self contained module. Three 30 dB, one 20 dB and one 10 dB pad are used whose frequency response is factory set. Each pad is operated by TO5 relays. 16 dB of fine level control is achieved using PIN diode attenuators.

Modulation

5. Amplitude, frequency and phase modulation can be provided internally from a 1 kHz modulation source which is derived from the instruments own internal frequency standard.

6. Amplitude modulation. For carrier frequencies greater than 62.5 MHz, modulation is obtained using PIN diode attenuators and envelope feedback. Modulation depths up to 80% are specified. At carrier frequencies less than 62.5 MHz a fixed frequency modulator operating at a frequency of 160 MHz allows up to 95% depth of modulation. AM is d.c. coupled.

7. Frequency modulation. FM is created by applying the modulation signal to varactor(s) in the 250 - 500 MHz oscillator. Simultaneous modulation of the reference frequency prevents fall off in response below the loop bandwidth. FM off (c.w. mode) gives the lowest residual f.m. noise. The low frequency response is tailored to optimize the modulation accuracy of low frequency square waves.

8. Phase modulation. This is achieved using a differentiator in the modulation signal path and then applying the treated signal in the same manner as the f.m.

9. Modulation signal a.l.c. This is always in circuit when internal modulation is in use and may be selected when switched to external modulation. The circuit uses a j.f.e.t. and allows up to 10% error in a 1 V input before a HI or LO message in the modulation display indicates that the applied modulation signal level is outside the range of the a.l.c.

Control

10. Front panel operation is carried out by direct entry of required settings via the keyboard. Microprocessor control ensures flexibility, simplicity of use and allows programming by the General Purpose Interface Bus (GPIB). This facility is offered as an optional accessory enabling the instrument to be used both as a manually operated bench mounted instrument or as part of a fully automated test system.

11. Both analogue and digital circuits are incorporated to control the instrument. Three methods of data transfer from the microprocessor to the remainder of the instrument are used.

(1) The v.c.o. frequency is set by direct parallel loading from the microprocessor to the synthesizer board.

(2) Analogue control of functions such as a.m. depth and r.f. level is maintained by first converting data into a serial format then transmitting it from the microprocessor/synthesizer box. The data is then converted back to an 8-bit parallel format which is loaded into Digital-to-Analogue Converters (DACs). This causes gain changes which vary voltage levels as appropriate.

(3) The third method is to convert the parallel data on the control board into a special serial format that is fed to the liquid crystal display drivers.

12. The microprocessor used is an 8085A and incorporates an 8-bit multiplexed data/low order address structure to allow a 16-bit address bus. 2 K bytes of RAM are used for temporary storage. 32 K bytes of EPROM are used for the instrument's operating programme (which should be considered as a read only memory) and 2 K bytes of non-volatile EAROM are available for user control settings and calibration information.

DETAILED TECHNICAL DESCRIPTION, SYNTHESIZER (AA1)

Circuit diagram : Chap. 7, Fig. 6

250-500 MHz synthesis

13. This is accomplished by fractional N synthesis and is made up of a system divided into three areas as follows:-

(1) 40 kHz synthesizer, a conventional type operating in 40 kHz increments and consisting of a fully programmable divider, a 40 kHz reference divider, a phase/frequency comparator and a loop filter.

(2) Fractional N accumulator whose purpose is to make periodic modifications to the division ratio of the synthesizer so that the average division ratio is a fractional value (i.e. interpolating between the 40 kHz increments).

(3) A jitter correction circuit whose function is to correct for the unequal spacing of the divider output pulses caused by the operation of the accumulator.

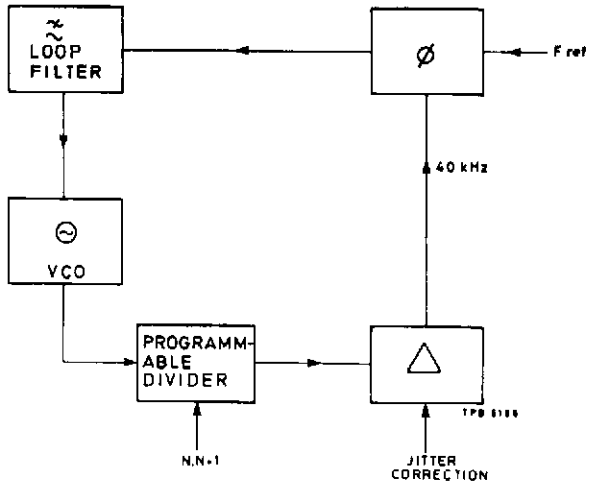


Fig. 1 Fractional N synthesis simplified block diagram

14. Fractional N synthesis. In single-loop synthesis, the minimum frequency increment attainable equals the reference frequency. Thus fine frequency increments can only be attained at the expense of a very low reference frequency. This requires extensive filtering at the loop filter, resulting in a low loop bandwidth and consequent poor performance. Fractional N synthesis overcomes this restriction.

15. Increments smaller than Fr are generated by making periodic adjustments to the division ratio so that the average value of division is actually a fractional number. The output pulses from the programmable divider no longer have a uniform spacing and this must be corrected before the signal reaches the phase comparator otherwise spurious modulation or 'jitter' will occur. The circuit that computes the adjustments to the division ratio also generates a correction voltage and this is used to delay the output pulses to return them to uniform spacing, eliminating the jitter.

16. 40 kHz synthesizer. The 10 MHz internal crystal oscillator X1 is divided down to 40 kHz by the action of IC2a, IC8a,b, IC14a, IC20b,c and fed to IC22 phase/frequency comparator. A 250 - 500 MHz input from AB1 RF processing board drives IC9 four modulus pre-scaler via PLX and C4. Internally this consists of two cascaded two-modulus 15/16 pre-scalers. Both normally divide by 16 giving a total modulus of 256. If IC9 pin 4 (control A) is taken to logic 'low', then in the following output cycle the first of the 15/16 dividers is set to 15 for just one count cycle. Thus the modulus is reduced to 255.

17. If IC9 pin 5 (control B) is taken 'low', then the second 15/16 divider is set to 15, however as this is preceded by the other divider (which is dividing by 16) then the modulus falls to 240. If both control pins 4 and 5, are taken low, the modulus falls to 239.

18. IC9 pre-scaler is used in conjunction with four programmable counters IC4,IC5,IC16 and IC17. The nominal modulus of the pre-scaler is 256 and so the data loaded into IC16/IC17, counter C, determines the number of times that 256 is counted. IC4 and IC5, counters A and B, modify the division ratio of the pre-scaler for some of the time.

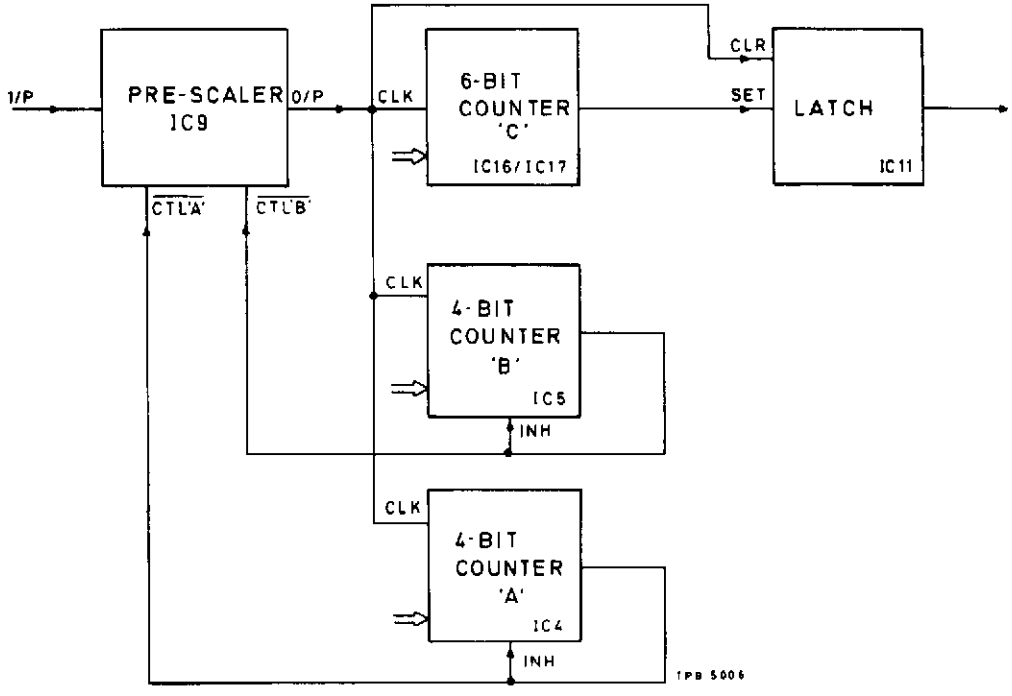


Fig. 2 Four modulus prescaler circuit (AA1)

19. Counter B is loaded with data that reduces the division ratio of the pre-scaler by 16 for anything up to sixteen output cycles of the pre-scaler. Counter A is loaded with data that reduces the division ratio of the pre-scaler by 1 for up to sixteen output cycles of the pre-scaler. Total division ratio is (256 x C) - (16 x B) - A so providing a division ratio that is fully programmable.

20. Operation, the data is loaded into the counters and if this is not zero the terminal count (TC) outputs of both A and B counters will be low and a modulus change is activated. IC9 pre-scaler output then clocks the counters IC4,IC5 (which are hard-wired to count down) and within sixteen counts 'A' and 'B' will reach zero, the two control lines will be returned to logic 'high' state and further counting is inhibited.

21. Counter 'C' continues to count until it too reaches zero and TC is taken to logic 'high'. This sets IC11b latch which in turn produces an output pulse to activate the LOAD inputs of all three counters. When the CLOCK line is next asserted to logic 'low' IC11b latch is released and the counters are ready to count on the next positive-going clock transition. IC16 and IC17 together form counter 'C' and IC11b combines both TC outputs to implement the latching function. IC17 TC goes 'high' first setting the D input, then IC16 TC follows, clocking the terminal count onto the output.

22. A fractional N synthesizer requires an additional control line that when activated causes the total division ratio to be changed by one. This line originates from IC27 pin 14. If this line is logic 'high' IC11a pin 1 will also be held 'high'. IC4 counter 'A' TC line is routed via IC10a and gated with the Q output of IC11a to the pre-scaler Control 'A' (CTA) line. This allows the option of holding the CTA line logic 'low' for an extra count and changing the division ratio by unity. Towards the end of a division cycle IC4 pin 12 will also be 'high' and IC11a pin 6 will be clocked 'low'. This activates the preset input and locks IC11a, pin 6, 'low'. IC10a pin 2 is therefore held 'high' and TC is effectively connected directly to IC9 CTA and the division ratio is unmodified.

23. If the line from IC27 pin 14 is low and IC11b produces a divider output pulse, this appears as a negative-going pulse on IC11a pin 1 and clears IC11a during the time that the counters are being loaded. IC10a pin 2 is now held 'low' and cannot return 'high' until IC4 pin 12 goes 'high' and the subsequent pre-scaler clock pulse is received. Thus the line to pre-scaler CTA is held low for one extra count and the division ratio is reduced by one.

24. Phase/frequency comparator, this comprises IC22 and IC20d. The output of the programmable divider is routed to IC22 pin 11 via a jitter correction circuit, (described later). If the leading edge of the pulse arrives before the reference divider pulse at IC22 pin 3 then the v.c.o. frequency is too high. IC22 pin 8 is then set 'high' and returns 'low' after the reference divider pulse is received on pin 3. TR8 conducts drawing current into the loop filter circuit IC28, causing the voltage at IC28 pin 6 to decrease. If the pulse from the programmable divider arrives after the reference divider pulse then pin 5 is set 'low' and TR7 conducts and raises the voltage at IC28 pin 6. R27 and C23 delay the resetting of the circuit by approximately 50 ns to maintain at equilibrium a finite pulse width to both TR7 and TR8. In this way phase response is improved (dead spots are avoided).

25. R35,C27 and C28 form part of the loop filter in conjunction with other components on AB1. Dividing the loop filter components in this way reduces the sensitivity to unwanted external pick-up and allows interconnections to be

made between AA1 and AB1 using ribbon cable. There are two output lines, VCO TUNE A is the output to AB1 via PLT pin 14, VCO TUNE B (PLT pin 13) is a dedicated earth return from AB1 to prevent the formation of a hum loop through the instrument chassis.

26. Fractional N accumulator, this system has an improved resolution of 4000 over the 40 kHz synthesizer previously described and gives 10 Hz increments. This is accomplished by making periodic modifications to the division ratio such that the average division ratio is the required fractional value. So in a sequence of 4000 output pulses from the programmable divider, the division ratio could be modified for 0 - 3999 of these periods. If the division ratio is modified from N to N+1 for M of the 4000 periods, then the average division ratio becomes N+M/4000 and the average output frequency becomes

$$\left[N + \frac{M}{4000}\right] \times 40 \text{ kHz}.$$

27. The purpose of the accumulator is to generate the sequence of division ratio modifications. The accumulator has a capacity of 4000 and is clocked from the output of the programmable divider. At each clock pulse the value M is added to the contents of the accumulator. When the accumulator overflows, a division ratio change is implemented in the next period. At the end of 4000 periods, the total number loaded into the accumulator will be 4000 x M and thus M overflows will have been created during this time. The overflow occurs with approximately uniform spacing considering that M may not be on an exact sub-multiple of 4000.

28. The output pulses from the programmable divider no longer have a uniform spacing because periodic changes have been made to the division ratio. If these changes are allowed to reach the phase comparator error signals would result and modulate the v.c.o. causing unwanted frequency jitter. This is prevented by the incorporation of a jitter correction circuit which is described below.

29. Jitter correction circuit. When M is unity or close to it this could correspond to a 10 Hz offset from a 40 kHz frequency multiplier. The programmable divider will be dividing by N for 3999 times and then N + 1 just once. This is seen by the phase comparator as a gradually increasing phase error that is occasionally pulled back to zero. This occurs because the correct division ratio is N+1/4000 and the N error is slight, the N+1 error however is much greater so that while the divider is dividing by N each successive pulse is arriving a fractional amount sooner with respect to the reference. When the N+1 division is implemented the pulses are brought back into line.

30. To return the pulses to a uniform spacing and prevent jitter involves the retarding of the programmable divider during the time it is dividing by N, then removing the retarding when the N+1 period is reached. The count resident in the accumulator is proportional to the amount of retarding needed and represents the phase error referred to the input of the programmable divider. As the accumulator fills the phase shift is increasing and the overflow occurs when one cycle of phase shift has accrued. The implementation of an N+1 division at this point effectively swallows that extra cycle, returning the phase shift to zero.

31. Jitter correction is implemented by feeding the contents of the accumulator into a digital-to-analogue converter. An output voltage proportional to the retarding is produced and is used to set the threshold on a comparator. A

second input is fed from a ramp triggered from the output of the programmable divider. The coefficient of the resultant voltage-to-time conversion is set so that the full swing of the digital-to-analogue converter produces a change equal to one cycle at the input of the programmable divider. This is in the range 250 - 500 MHz resulting in timing changes from 4 to 2 ns from which the required coefficient is inversely proportional to the synthesizer frequency and is accommodated by varying the reference voltage to the digital-to-analogue converter.

32. Operation, IC25-IC27 form a 12-bit full adder. The value M referred to in previous paragraphs is latched into IC23 and IC24. IC31 and IC32 form a 12-bit edge-triggered data latch. IC29 and IC30 can be assumed to be transparent in this instance. Feedback from IC31 and IC32 to the input adders IC25-IC27 form an accumulator. Each time the latches are clocked (IC31,32 pin 9) the new output is summed with M and the result presented back to the input of the latches. Overflow, when it occurs, appears at IC27 pin 14.

33. The accumulator is required to overflow at 4000 and not 4096 which would normally be the case. This is achieved by IC29 and IC30. An overflow causes IC29 pins 3 and 5 to go to logic 'high' and this adds 96 to the number fed back to the latch. The size of the accumulator is thus effectively reduced to 4000 although all the output numbers are 96 higher than normal. This is of no consequence as only the relative phase of the correction signal is important. The overflow line (IC27 pin 14) is fed back to the programmable divider where it implements the division ratio change previously described. IC33 is a multiplying digital-to-analogue converter, the frequency dependent reference voltage arriving on pin 15 via PLT pin 1. This reference is generated on A2 board.

34. The jitter correction circuit comprises C50 normally shunted by TR9. When the programmable divider outputs a pulse TR9 base is taken low and C50 charges via R39 and L4. A ramp is generated with a duration which is sufficiently brief that the current in L4 remains reasonably constant and the ramp linear. When the voltage exceeds the voltage from the digital-to-analogue converter by 0.6 V, TR10 conducts and an output pulse is produced to trigger the phase comparator. The greater the voltage from the digital-to-analogue converter, the longer the time delay.

BFO phase locking

35. The 160 MHz oscillator on AB1 board is locked to the 10 MHz frequency standard. The circuit comprises a fixed ratio divider (modulus 16), a phase /frequency comparator and a loop filter. The 160 MHz signal is fed to IC1 pin 1, via PLU pin 1. IC1 pin 8 is biased to prevent self-oscillation of IC1 in the absence of a signal. Output is fed to IC6 pin 3 and a 10 MHz reference to pin 11.

36. The circuit functions in a similar manner to IC22 but because the frequency is higher Shottky t.t.l. is used and the feedback delay components are omitted. IC6 outputs on pins 5 and 8 turn on TR1 and TR2 respectively. C10,C12 and L1 form a low-pass filter to prevent the feedback of 10 MHz components to AB1. The loop filter itself is on AB1 board.

Crystal oscillator (internal/external locking)

37. External standard operation is accomplished by phase-locking of the internal 10 MHz crystal oscillator rather than by its substitution with the

external signal. The method effectively eliminates spurious signals that may be present on the external standard. A further advantage is that if gross frequency errors occur in the external standard or if it fails completely, this would be flagged as an error condition but the instrument will continue to function on the internal oscillator.

38. External standard is fed via PL5 pin 1 to the Schmitt trigger IC34 pins 1 and 2, R5 assisting in terminating possible reflections. When EXT STD is selected, IC2 pin 2 is set 'high' allowing the signal to reach IC7 pin 11. The crystal oscillator output is divided to 5 and 1 MHz by IC8a and either 10,5 or 1 MHz (dependent on the link setting) is routed to IC7 pin 3 which, like IC6 and IC22, is used as a phase-frequency comparator. Links can be reset as described in Chapter 5 Maintenance. TR3 and TR4 outputs are summed across C15 which together with R1 and the rear panel frequency adjustment form the loop filter. When INT STD is selected no clock pulses arrive at IC7 pin 11. In this condition pins 5 and 8 are static and both TR3 and TR4 are turned off. The voltage on crystal oscillator X1 pin 5 is now determined solely by the setting of the rear panel adjustment. When selected to EXT STD pulses are coupled to the emitter of TR3 or TR4 depending on the direction of phase error, and their output voltage fed to the crystal oscillator, to achieve phase lock.

39. Two detection circuits are incorporated to prevent incorrect operation. D5,D6,C13 and C14 form a signal detection circuit. IC15 pin 1 only goes to logic 'high' when a signal is present at IC34 pin 3. IC12b and IC12c together with D8 and D9 form a window comparator. If operation with an external standard causes the crystal oscillator tuning voltage to fall below 1 V, or rise above 10 V, IC15 pin 2 will be set to logic 'low'.

40. When EXT STD is selected, IC2 pin 2 is taken 'high'. The sense of the EXT STD VALID line is tested (IC15 pin 3) and if this is logic 'low' operation is correct. If it is 'high' this would indicate that the external standard has either an incorrect level, incorrect frequency or is non-existent. In this condition the processor takes IC2 pin 2 to logic 'low' and returns the instrument to INT STD. The sense of IC15 pin 3 is again tested. If this is still 'high' then the signal is not being detected and therefore is either non-existent or at too low a level. If however the sense of IC15 pin 3 is logic 'low' then it is the signal frequency that is incorrect. The appropriate error message is displayed and the testing sequence continued until either correct operation is detected or the instrument is returned to INT STD by the user.

Angle modulation at low frequencies

41. The 250-500 MHz synthesizer has a loop bandwidth of approximately 200 Hz giving the best compromise between switching speed and reference breakthrough. Inside this bandwidth f.m. applied solely to the v.c.o. will be attenuated due to the loop error correcting action. Since it is necessary to replicate a 10 Hz square wave, the response must be extended below that of the v.c.o. phase locked loop. To achieve this the f.m. is effectively applied to the reference side of the loop in the same sense as that applied to the v.c.o. and with the same deviation expressed as a percentage of its frequency. This means that no error signal is produced at the output of the phase frequency comparator and the f.m. is successfully implemented.

42. When f.m. or ϕ.m. is selected the 40 kHz reference is routed via a phase modulator comprising TR5,TR6 and IC18. IC14 pin 7 produces a positive-going pulse and this turns on TR6 discharging C17. TR6 then turns off and C17 is

charged via TR5 which is a current source. When the voltage on IC18 pin 2 exceeds that on pin 3, pin 7 goes to logic 'high' and in turn clocks the reference input of IC22, phase frequency comparator. The time delay thus produced is in proportion to the voltage applied to IC18 pin 3.

43. The f.m. signal is processed on A2 board and this is scaled and integrated so as to represent the degree of phase modulation required. It is then applied to IC18, pin 3 via PLT pin 10. In c.w. operation, IC20 pin 2 is taken to logic 'low' and pin 13 logic 'high'. The 40 kHz reference is now routed from IC14 pin 6 through to the phase comparator and the modulator is bypassed. This ensures the best possible noise performance in the c.w. mode.

1 kHz internal modulation tone

44. The 40 kHz reference at IC14a pin 6 is further divided by IC8a and IC14a to give a 10 kHz output at IC14a pin 3. This output is fed to IC14b wired as a bi-quinary counter which in turn divides the signal down to a frequency of 1 kHz at pin 13. The signal is then filtered by IC21a and IC21b configured as a four-pole Sallen Key low-pass filter, with the output level being set by R43. IC14b is disabled when the internal tone is not required to prevent the breakthrough of 1 kHz into the modulation circuits.

MICROPROCESSOR (AA2)

Circuit diagram : Chap. 7, Fig. 7

45. The microprocessor controls the flow of data necessary to drive both address and data bus lines. Information from the keyboard or the GPIB is received to control such functions as RF level, Modulation depth and Carrier frequency. Transmission of data to the appropriate latches may either be direct onto AA1, or via a serial link to A2. Functions of the board are divided into the following areas:-

(1) Microprocessor
(2) Address decoding
(3) Serial bus transceiver
(4) RAM, PROM and EAROM memory
(5) Timer
(6) Memory protection and +21 V EAROM supply
(7) Synthesizer driver

Microprocessor (IC2)

46. The 8085 Microprocessor IC2 has an 8-bit multiplexed data/low order address structure to allow a 16-bit address bus. The 8 least significant bits of the address bus are demultiplexed by the latch IC3. IC2 is clocked on pin 1 by a 5 MHz signal and is divided internally to provide two non-overlapping 2.5 MHz phases.

47. Three restart lines (or interrupts) are available. RST 7.5 is positive edge triggered and handles most of the instrument interrupts such as GPIB, keyboard, RPP and modulation HI/LO signals. These are described in A2 board technical description. RST 6.5 and RST 5.5 are level controlled (logic 'high' causing a jump). RST 6.5 is fed from AA1 synthesizer board and will go 'high' if the external frequency standard when selected, is not valid. RST 5.5 is used for the timing process monitoring the instrument's elapsed time.

48. A number of test points available on the board (TP3-TP12) are only used when factory testing the board initially. Two lines that are normally used for serial data transmission are available, SID and SOD on pins 4 and 5. In this application SID monitors the state of the EAROM, IC10, whilst SOD allows the timer to operate correctly. The RESET L (pin 36) is an input which if taken 'low' will cause the processor to jump to the initializing routine when the RESET line on pin 3 is taken 'high' again. This facility is used to prevent spurious addressing of any memory locations during power failures.

Address decoding

49. The 8 least significant bits (A0 - A7) of the address are de-multiplexed from the data/low order address bus. This is carried out by IC3. When the address enable line (ALE) is taken 'high' data present on IC3 pins 3,4,7,8, 13,14,17 and 18 are latched onto the corresponding outputs of IC3. The data bus can then be used to read or write information to the appropriate location dependent on the state of the RD L and WR L lines on IC2 pins 31 and 32. The appropriate location could be any memory IC or one of a number of latches used to interface between boards.

50. IC4 provides further address decoding for the three most significant address bits. RESET line, pin 4 ensures that the outputs of IC4 are disabled if the +5 V rail falls below +4.5 V. All outputs will be set 'high' if TP2 goes 'low' or pin 4 goes 'high'.

Serial bus transceiver

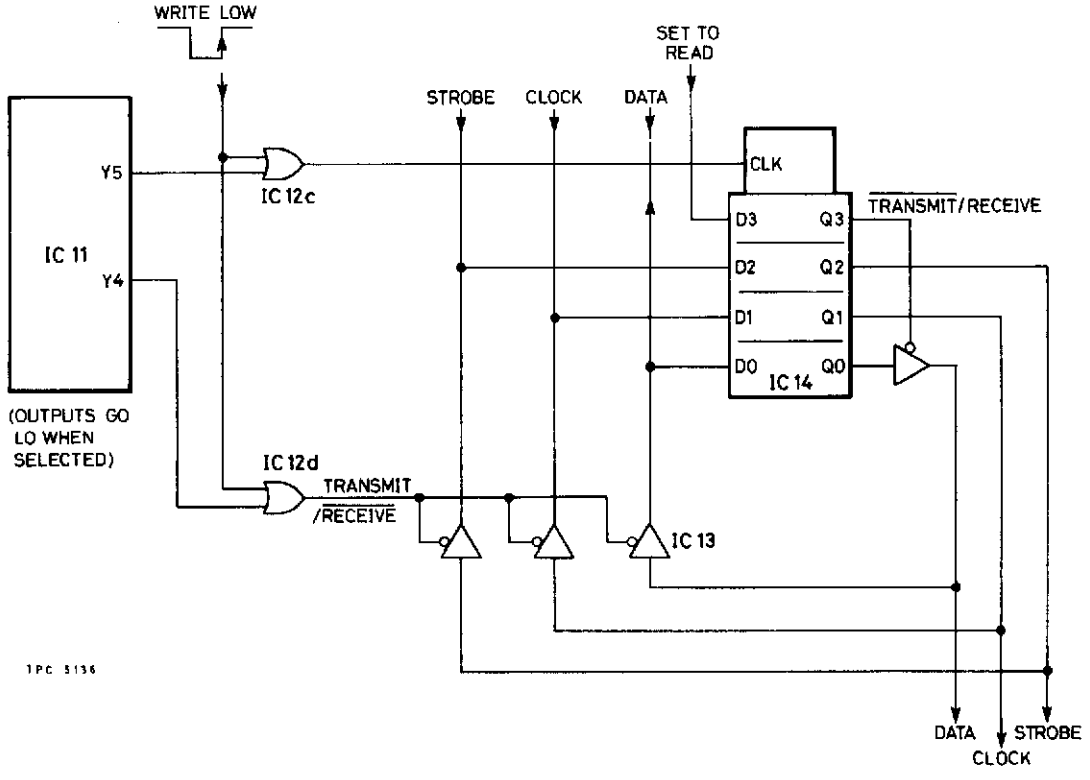


Fig. 3 Serial data transceiver (AA2)

51. This arrangement is used to communicate with all devices mounted outside the RF box AA0. Plug PLAC carries three lines to effect data transfer, see Fig. 3. These are pin 4, CLOCK, pin 5, STROBE and pin 6, DATA. The DATA line is bi-directional whilst the CLOCK and STROBE lines only carry information out from the microprocessor board. The +5 V supply rail and the RST 7.5 INTERRUPT line together with an earth are the remaining connections made via PLAC.

Data transmission

52. To obtain the required sequence, information is set up one bit at a time on the data line, then the CLOCK line is asserted 'high'. The positive edge of the CLOCK pulse will enable the shift registers on A2 board to accept the data. The STROBE line will be taken 'high' to transfer data entered in this manner to the registers when appropriate. Fig. 4 shows the basic circuit arrangement for data transmission.

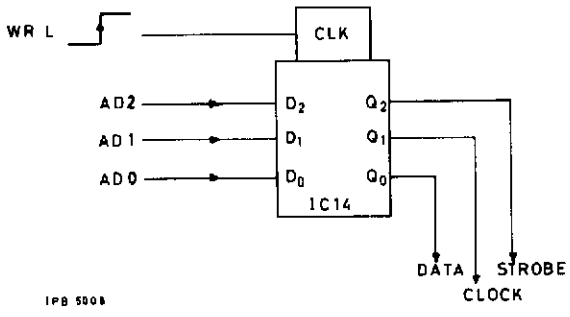


Fig. 4 Data transmission (AA2)

53. IC11 is configured to appear as a part of the memory space and is written to when data is to be clocked into IC14. Taking IC11, pin 10 'low' allows the WR L from the microprocessor to pass through IC12c to the clock line of IC14. IC12 routes those WR L signals for which address lines A0 and A1 are decoded to define one of four paths. For serial data transmission A1 is 'low' and A0 is 'high'.

54. After a data bit has been written onto the DATA line (PLAC, pin 6) a clock edge is generated by writing a different word to IC14. This byte consists of 02H for the clock information and 01H or 00H for the data information, the latter determines what goes into the latches on A2.

55. **STROBE.** If data just sent is to be latched onto the outputs of A2, IC5, IC7 and IC9, a byte equal to 04H will be written to IC11's address. This will cause IC14, pin 5 to be taken 'high' and that level will be clocked through. This will take the STROBE line of all latches 'high' allowing the data present at that time to be transferred to their outputs.

Data reception

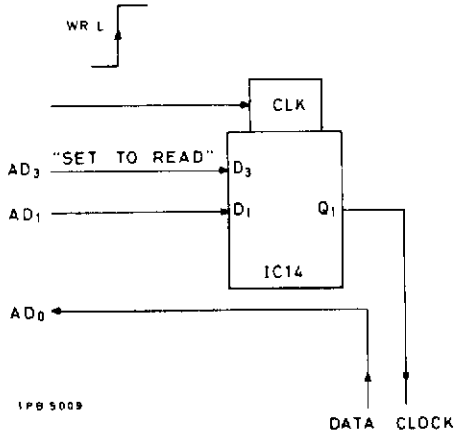


Fig. 5 Data reception (AA2)

56. In order to send information from A2, to AA2, microprocessor, data is clocked out from an eight bit shift register into a memory location in the processor's memory space. By rotating the bit addressed in the latter the serial to parallel conversion can take place. To realize this the arrangement on AA2 is slightly altered. Fig. 5 shows how this occurs. IC14, pin 2 is taken 'high' which disables IC13d. IC13c pin 13 is taken 'low' when appropriate to allow the data from A2 to have control over the data/address line AD0.

57. IC14 pin 10 is the CLOCK output whose positive edge will be used to cause a further data bit to come from A2, IC8, Q8. This is achieved by sending a 'high' level to IC8 pin 10 via IC5,IC6a and IC26c. The data bit, entering at PLAC pin 6, is read into a RAM location from where it may be addressed for further use.

Memory

58. **RAM,** IC9 is a 2 K byte (1 K = 1024) static CMOS RAM chip which is used as a temporary store for the intermediate stages in calculations such as Level conversion from dBm to µV.

59. **EPROM,** IC5,6,7 and 8 form a 32 K byte store for the instrument's operating programme. Each integrated circuit is an 8 K byte ultra-violet erasable read only memory. All are programmed during initial manufacture and should be considered as a read only memory.

60. **EAROM,** IC10 provides 2 K bytes of non-volatile memory and stores data which includes calibration information and control settings entered by the user. In order to write into or erase IC10 a supply of +21 V is made available to pin 1. However to avoid accidental corruption of the stored data two protection schemes are incorporated, one of these is written into the instrument's software and is described in the second function details. The other is a hardware circuit, "memory protection" which is described in later paragraphs. IC10 pin 2 SID line is used to inform the microprocessor when a write command has been executed (otherwise an unacceptable delay would be experienced when addressing a normal memory location).

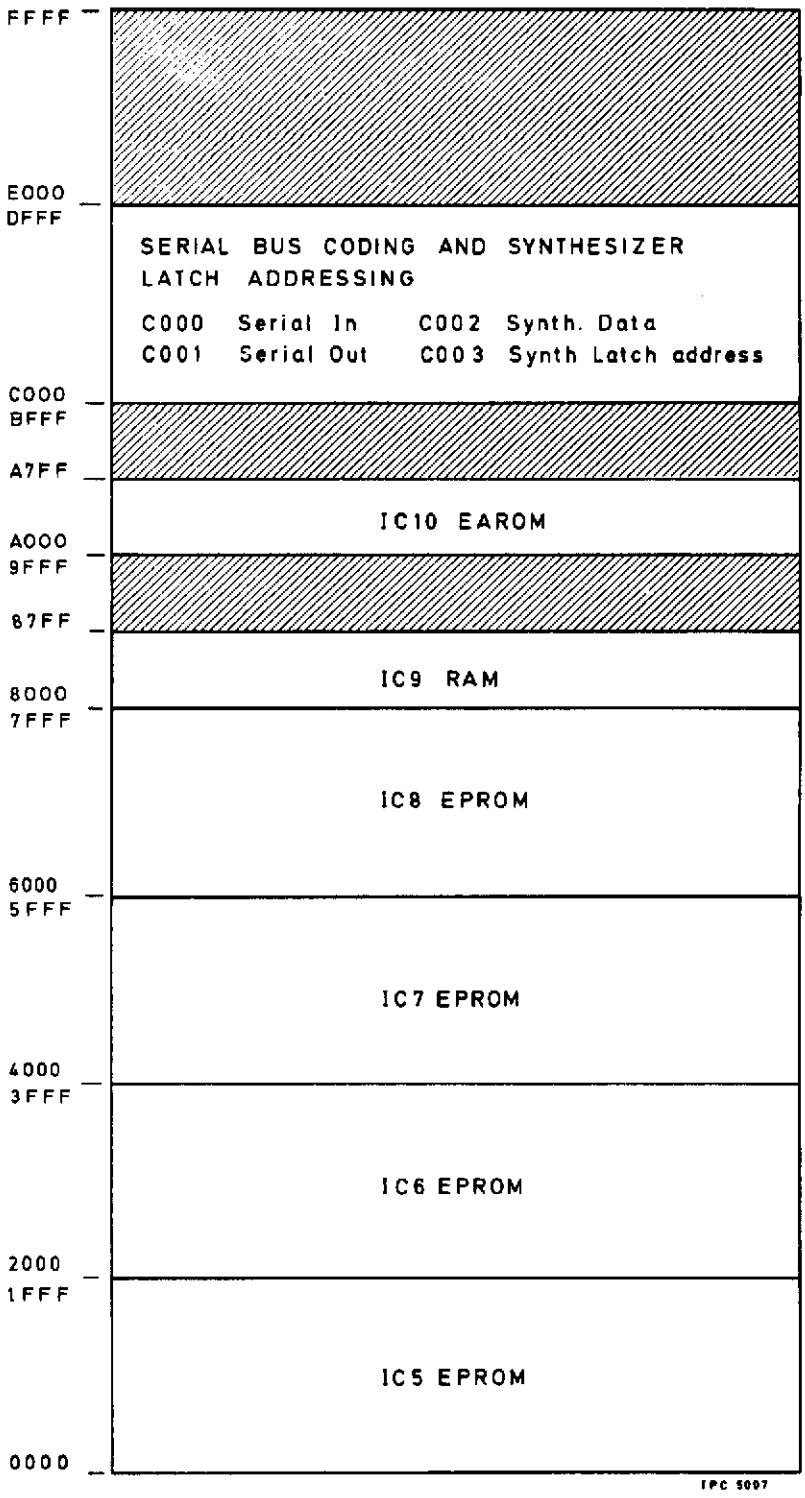


Fig. 6 Allocation of memory space (AA2)

Timer

61. Allowance is made in this circuit for the user to monitor the instrument's total number of running hours to date. This timing facility is particularly useful when recalibration periods are to be determined after a given number of hours. IC17, IC18 are used as dividers to allow sensibly long timing intervals to be achieved. IC17 is configured as an eight bit counter which then feeds IC18 a fourteen bit counter. This in turn causes a level triggered interrupt (RST 5.5), when its output is set 'high'.

62. IC17 and IC18 count to $\approx 2.1 \times 10^6$ and the RST 5.5 INTERRUPT occurs every ≈840 ms. Each interrupt clocks a further software counter until after a 15

minute period a new entry is made to data in the non-volatile memory of IC10. Two elapsed time readouts correct to within 30 minutes can be observed on the front panel display via second functions 9 and 198.

Memory protection and +21 V EAROM supply

63. To ensure that the integrity of data in the non-volatile memory is maintained it is essential that there is no risk of writing to it whilst the microprocessor is not completely functional. This can occur if the +5 V rail falls to some undefined level. In this event IC1 and its associated circuit will come into operation.

64. IC1b is a comparator that compares the +5 V rail with a voltage derived from the +24 V divider chain R3, D2, R17, R2 and R1 (SET +21 V). D1 and D4 protect the inputs of IC1. Normally the output of IC16 will be 'low' since IC1b, pin 5 will be at a nominal +4.5 V. No current will flow through R9 and so TR2 will be switched off. R11 will cause the RESET L line to assert 'high' to allow the correct instrument operation.

65. If the +5 V rail temporarily, or permanently, falls below +4.5 V, TR2 will turn on causing the microprocessor to jump to a pre-defined memory location. If the rail returns to more than 4.5 V the 2022 will merely re-initialize itself as if power had again been applied. C3 and R11 have a time constant that will tend to prevent multiple resetting of the microprocessor.

66. As the output of IC1b goes 'high' D5 will turn on causing the non-inverting input of IC1a to rise above the inverting input. IC1a pin 1 will therefore switch 'high', D3 (normally acting as a ZENER) will stop conducting and TR1 will be turned off. The +21 V rail will no longer reach IC10 thus preserving the stored data and preventing corruption.

67. Under normal circumstances IC1a acts as a comparator of the reference provided by resistors R12,R13,R17 and a proportion of the +21 V used to drive IC10. R7 and R4 are chosen to give +4.5 V at their junction. IC1a, pin 1 changes level until sufficient current is being drawn through D3 to set the operating point of TR1 such that +21 V is present on its collector. C2 absorbs discharge transients when IC10 is being written to.

Synthesizer driver

68. AA1, Synthesizer board requires 26 bits of data to set the oscillator frequency (2^{26}x10 Hz ≈671 MHz which is the nearest factor to 500 MHz) and 4 bits of control data. AA2, IC15 and IC16 allow this data to be transferred from the microprocessor to the synthesizer. IC15 acts as an address latch whilst IC16 controls six data lines on PLAB, pins 5-10.

69. Both of these latches are configured as part of the memory address space, see Fig. 5, and are merely written to when frequency data is to be updated. IC11 provides the address decoding and controls the routeing of the WR L path through IC12a and b. A positive edge transition on IC15 or IC16, pin 9 will transfer input data to the outputs.

RF PROCESSING BOARD (AB1)

Circuit diagram : Chap. 7, Fig. 8

70. This board houses the entire RF generation system and is comprised of five signal generation circuits briefly described as follows:-

(1) 250 - 500 MHz - A conventional v.c.o. system employing two oscillators, each one operates over a half octave with a changeover point at 353 MHz. A tunable notch filter reduces second harmonic content of the output.

(2) 62.5 - 250 MHz - This frequency range is obtained by dividing down the v.c.o. frequency range with the divide-by-two networks. Low-pass filters are employed to reduce the harmonic content.

(3) 500 - 1000 MHz - The v.c.o. output is fed to a frequency doubler circuit which comprises a balanced transformer and diode bridge. Insertion loss is compensated for by an additional amplifying stage. A voltage tuned band-pass filter enables sub-harmonic and harmonic components to be reduced.

(4) 62.5 - 1000 MHz output stage, this stage provides an automatic levelled output over the range +6 dBm to -10 dBm and also the means of d.c. coupled amplitude modulation up to a depth of 80% and specified for carrier frequencies 62.5 - 400 MHz. The output is converted to a 50 Ω source and fed to a relay selecting either this output or that of the b.f.o. system.

(5) 10 kHz - 62.5 MHz b.f.o system. a phase locked 160 MHz v.c.o. signal is used as one input to an r.f. mixer. Amplitude modulation is superimposed on this signal before mixing with a signal in the range 160.01 to 222.5 MHz derived from the output of the first divide-by-two network. The i.f. output of the mixer 0.01 - 62.5 MHz is then filtered to remove unwanted mixer products. A final amplifier stage provides a voltage gain of 26 dB and acts as a 50 Ω source. The output level is also peak detected and fed back to an input error amplifier to provide atuomatic level control and allow d.c. coupling of the amplitude modulator.

VCO system (250-500 MHz)

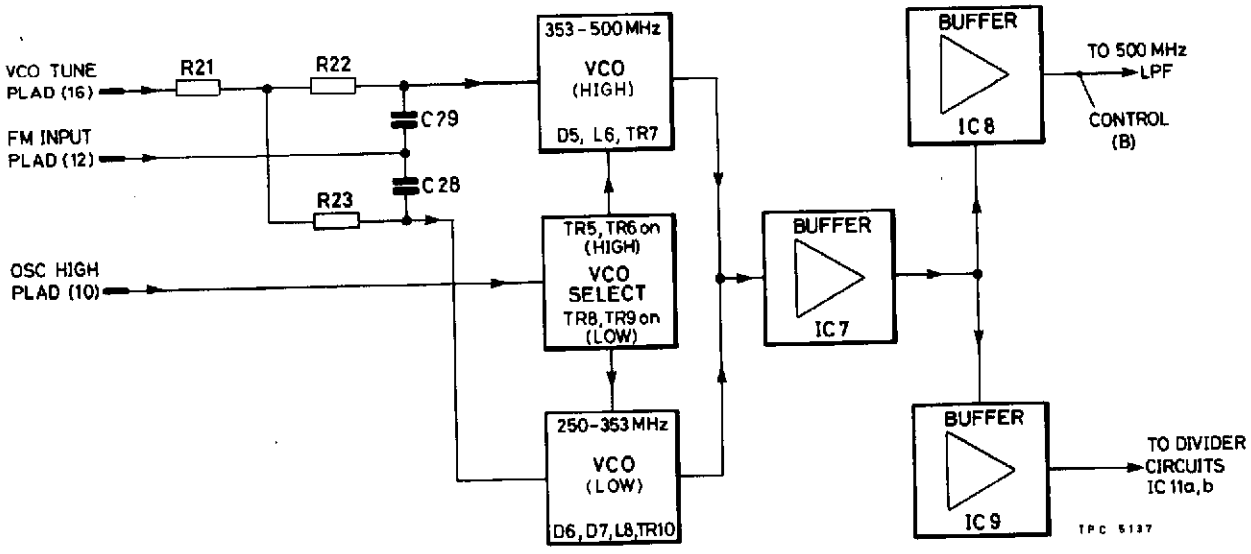


Fig. 7 250-500 MHz v.c.o. system simplified block diagram (AB1)

71. Two oscillators are used to cover the basic frequency range each one generating one half octave. Changeover occurs at 353 MHz. The upper half octave 353 - 500 MHz is generated from a tuned circuit formed by C31, D5, and L6, the latter is only evident as a thicker length of track on the p.c.b. The base of TR7 oscillator is driven from the centre tap of L6 and the collector via C37 and R34, these components are positioned so as to be mutually coupled to the oscillator tuned circuit.

72. R32,R33,C33 and C34 control the impedance of oscillator TR7 and compensate for unwanted internal phase shift within the transistor. Having resistors in both emitter and collector circuits also prevents the formation of parasitic resonance which would otherwise occur via the transistor's junction capacitances.

73. Tuning of the oscillator is carried out by the varactor D5 with bias applied via L5. The l.f. end of the oscillator range may be adjusted by C31 for 2 V at 353 MHz. The h.f. end of the range should be approximately 15 V at 500 MHz. Output is taken from a low tapping point on L6, via R27.

74. The lower half octave oscillator 250 - 352 MHz operates in a similar manner with the capacitor values doubled in the tuned circuit to give the half-octave reduction in frequency.

75. Selection 353 - 500 MHz (HIGH) and 250 - 352 MHz (LOW) is carried out by the OSC HIGH control line (PLAD pin 10) from A2 Control circuit. When this is asserted 'high' TR5 and TR6 conduct and complete the -12 V supply line to allow TR7 to conduct. When the OSC HIGH control line is at logic 'low' TR8 and TR9 conduct and TR10 is powered. Because only one oscillator is powered at a time from the single control line outputs are resistively summed at the input of IC7 amplifier. Both oscillators and amplifier are mounted within the on-board screening so as to achieve a very low level of load reaction.

Frequency dividers (62.5 - 250 MHz)

76. The v.c.o. output range (250 - 500 MHz) is divided into three paths via IC8, IC9 and IC10 buffer amplifiers. IC8 provides the signal path for the 250 - 500 MHz range, IC9 the 62.5 - 250 MHz range and IC10 provides a synchronizing output to AA1 programmable dividers.

77. Selecting of the required signal path is controlled by IC4-IC6 signal gating circuit. The control data is input via PLAD pins 6,7 and 11 and is shown on the circuit diagram as range control logic and uses the letters (A) to (G) to indicate where assertion of data (negative true logic) is made.

78. The output from IC9 drives two binary frequency dividers IC11a and IC11b. These D type flip-flops are wired as two binary dividers by connecting the Q outputs to their respective D inputs. The first divider is clocked via pin 11. Both Q and $\overline{Q}$ outputs are utilized, driving opposite ends of T1 balancing transformer. The output is taken from a third winding via D15 when control logic line (B) is asserted. This arrangement gives a symmetrical output waveform containing little second harmonic therefore simplifying filtering.

79. When (F) is asserted 'low' R59 and R61 provide bias to allow IC11a divider to operate. R58 and R60 provide bias to the clock inputs via L16 and L35 to maintain these at the mean logic level. The second divider operates when the bias provided via R78 and R79 is applied, this occurs when both (A) and (F) are asserted 'low'.

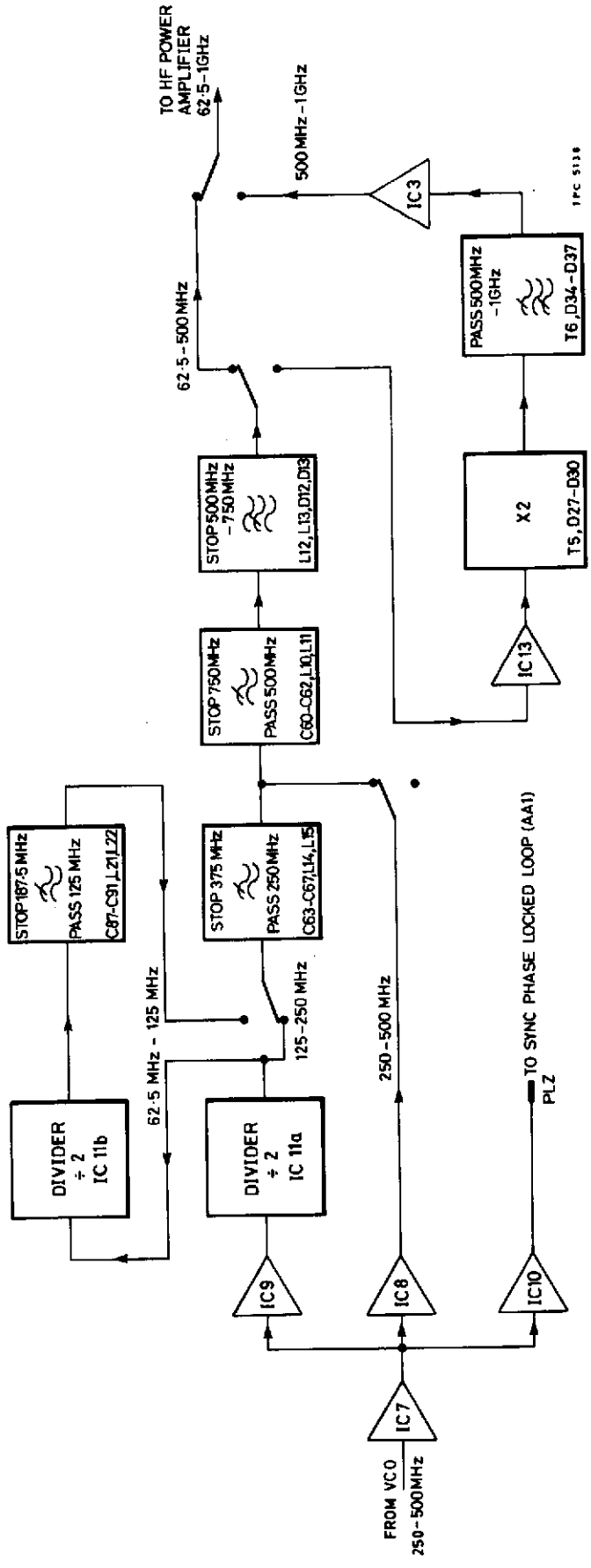


Fig. 8 Frequency dividers, simplified block diagram (AB1)

80. 250 - 500 MHz. When frequencies in this range are selected point (E) is taken 'low' turning D8 and D9 on and D10 off. (F), (A) and (B) are taken 'high', disabling IC11a,b dividers; D11 is also turned off. The signal path is then routed from IC8 and through a 500 MHz low-pass filter comprising L10,L11,C60-C62. Cut off frequency of this filter is 750 MHz enabling signals of up to 500 MHz to pass but none of the third or higher harmonics. A further tunable notch filter L12,L13,D12 and D13 eliminates the second harmonics in the range 500-750 MHz.

81. 125 - 250 MHz. When frequencies in this range are required point (E) is taken 'high', D8 and D9 are turned off and D10 is turned on. Points (F) and (B) are taken 'low' activating IC11a first divider. D11,D14 and D15 are also turned on and D17,D18 are turned off. The first dividers output is routed via D15 and D14 to a 250 MHz low-pass elliptic filter comprising L14,L15, C63-C67. Cut off frequency of this filter is 375 MHz so the required range is passed but the third harmonic in the band 375 - 750 MHz (and higher harmonics) are eliminated. The signal is then routed from the low-pass filter via D11 to the input of the 500 MHz low-pass filter to be combined with the 250 - 500 MHz signal frequency range.

82. 62.5 - 125 MHz. When frequencies in this range are required points (A) and ($\overline{F}$) are taken 'low' and (B) is taken 'high'. D15 is turned off, D16 and D18 are turned on, both IC11a and IC11b dividers operate and the output (62.5-125 MHz) is taken from T4 transformer secondary. The signal is passed through a 125 MHz low-pass filter L21,L22,C87-C91. Cut off frequency of the filter is 187.5 MHz to eliminate the third and higher harmonics. This allows the required 62.5-125 MHz band to be routed via D16 to the 250 MHz low-pass filter L14,L15. The signal is then combined with the 125-250 MHz and the 250 -500 MHz signal paths as far as the junction C71,D20,D21.

83. At C71 the signal paths divide. When signals in the range 62.5-500 MHz are selected point (C) is taken low and point (D) is taken 'high', D20, D23 and D31 are turned on and D32 is turned off, signals are routed to the input of the h.f. output amplifier stage via D20,D23,D31 and C102.

Frequency doubler (500-1000 MHz)

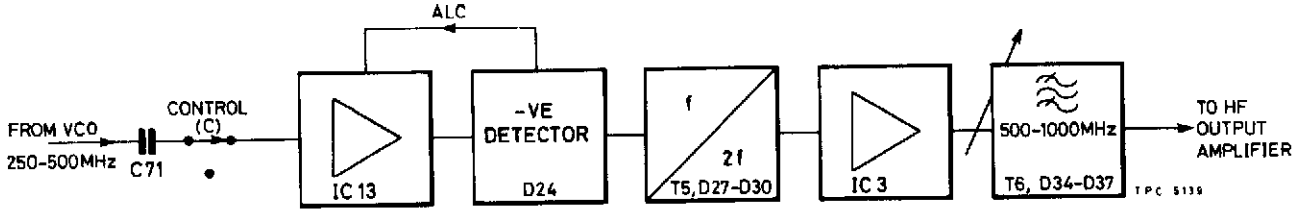


Fig. 9 Frequency multipliers, simplified block diagram (AB1)

84. The frequency range of 500 - 1000 MHz is obtained by taking the v.c.o. output range (250 - 500 MHz) from the output of the 500 - 1000 MHz notch filter and following this with a frequency doubler circuit. Selection is effected by the assertion of the range control logic, point (C) is taken 'high' and point (D) is taken 'low'. D20 is turned off and the signal path is then taken via the amplifier IC13. Output from IC13 is detected by D24 which drives an automatic level correction circuit. This controls the r.f. resistance of D21,D22 and thus the drive to the doubler circuit.

85. The frequency doubler circuit comprises T5, balancing transformer and D27-D30 diode bridge. Insertion loss of the doubler is compensated for by IC3 which provides 12 dB of amplification. This output is filtered by a 500 - 1000 MHz voltage tuned band-pass filter comprising D34-D37 and T6.

86. The filter together with the 500 - 1000 MHz voltage tuned notch filter previously described share a common control line. This originates from a digital-to-analogue converter on A2 board via PLAD pin 15. Tracking data is set by the requirements of the band-pass filter which has no other means of adjustment. The notch filter is then aligned to this data by adjustment of L13. Output from the 500 - 1000 MHz band-pass filter is connected via D32 and C102 to the h.f. output amplifier.

HF output stage (62.5-1000 MHz)

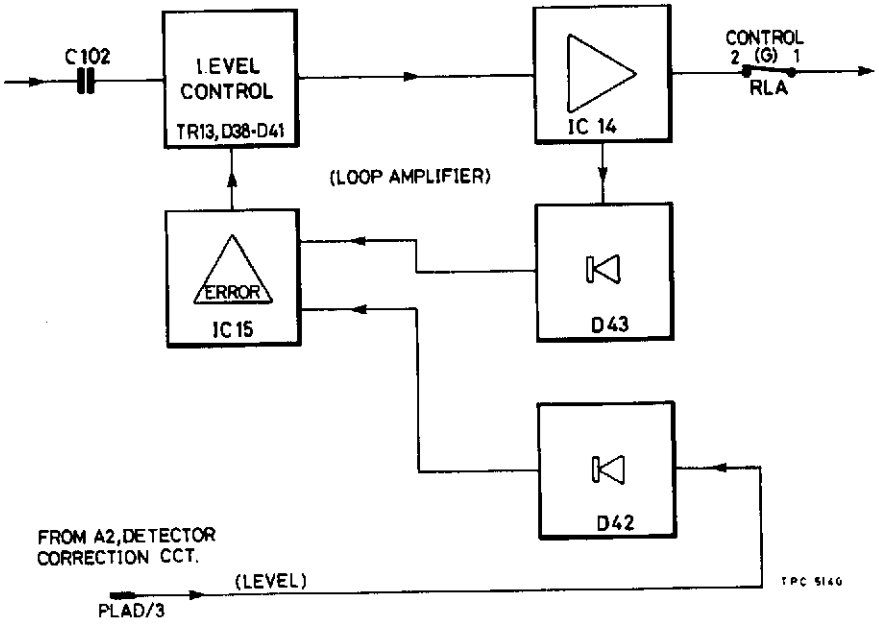


Fig. 10 HF output stage (62.5 - 1000 MHz) simplified block diagram (AB1)

87. The HF output amplifier stage comprises IC14 together with D43 output detector, loop amplifier IC15,TR13, and pin diodes D38-D41. The stage is required not only to provide levelled output over the range +6 to -10 dBm but also amplitude modulation of up to 80%. The total dynamic range of the a.l.c. is thus +6 to -24 dBm. AM is specified using carrier frequencies up to 400 MHz although the circuit is usable to 1000 MHz.

88. The r.f. reference level is fed to IC15 pin 2 via D42. D42 and D43 are in close thermal contact and operate at similar bias currents so that the voltages dropped across the diodes are accurately matched. IC15 pin 6 goes negative turning on TR13 and D38-D41. The r.f. output of the amplifier IC14 pin 8 rises until the peak voltage detected by D43 equals the reference voltage. When a.m. is in use the modulating voltage is superimposed upon the reference. This is performed on A2 board and is described in that section.

89. The levelling achieves a defined r.f. voltage at the input of R123 which provides a 50 Ω source. The output is then fed to relay RLA where point (G) range control logic selects either this output or the output from the BFO system.

BFO system and LF output stage (10 kHz - 62.5 MHz)

90. When frequencies between 0.01 - 62.5 MHz are required point (G) is at logic 'high' causing relay RLA to be de-energized. The relay has two contacts, one contact completes the +12 V supply to the oscillator, modulator, mixer and 1.f. amplifier, the second contact connects the 1.f. amplifier to the output attenuator AC0 via PLAE.

91. TR1 and its associated components form a Colpitts oscillator operating at 160 MHz. D1 provides the means of phase locking the oscillator. The phase lock loop is mounted on AA1 synthesizer board and control is effected via PLAD pin 1. TR2 provides a reasonably constant 3 mA bias current.

92. The output is buffered by IC1, both this and the oscillator components are contained within pockets in the on-board screening. The output from IC1 drives IC2 providing further isolation for a synchronizing output to AA1 board. IC1 also drives the fixed frequency amplitude modulator, TR3 and TR4.

93. These are configured as a long-tailed pair with TR4 collector components providing a tuned load. Current of both transistors is varied by the a.m. signal from A2 and at the same time both are switched at 160 MHz by the input applied to TR3 base. An amplitude modulated signal at 160 MHz is thus developed across L2, C18. Subsequent mixing and levelling operations do not affect the a.m. depth but serve merely to alter the carrier frequency and the overall signal level.

94. D2,D3 and D4 form a current-controlled attenuator, D3 provides a reasonably constant load and D4/C20 maintain effective attenuation of harmonics. L3,L4, C24-C26 form a 160 MHz low-pass filter. This together with the tuned load in TR4 ensures that the 160 MHz signal fed to X1 has a very low level of harmonics therefore ensuring good intermodulation performance.

95. The local oscillator drive to X1 covers the frequency range 160.01 to 222.5 MHz, this produces 10 kHz to 62.5 MHz at X1 mixer output. This local oscillator drive is derived from the output of the first frequency divider IC11a, and IC13 is utilized to boost the signal level. Point (D) is taken 'high' turning D16 off. D25 is turned on by the +12 V supply to the b.f.o. circuit. This routes the signal from IC13 to X1, R71-R73 form a 3 dB pad to absorb mis-matches.

96. The output of X1 is fed through a low-pass filter. Part of this, R70, C79 and L20 presents a termination to the mixer in the stop band. The complete filter (including C92, C93 and L23) passes 62.5 MHz but rejects 97.5 MHz (the lowest third order intermodulation product). This filter is terminated by R83 and is followed by the 1.f. output amplifier, TR11, TR12.

97. The 1.f. output amplifier provides a voltage gain of 26 dB. The output level is detected by D33 which, with C106, forms a peak detector. The lowest carrier frequency is 10 kHz so the detector time-constant required is a long one. When a.m. is present the detector measures the peak of the a.m. envelope; at 100% depth this will be double the voltage at 0% depth. To ensure that the r.f. level is still correct the reference voltage is increased by an amount equal to the detector voltage increase due to the a.m.

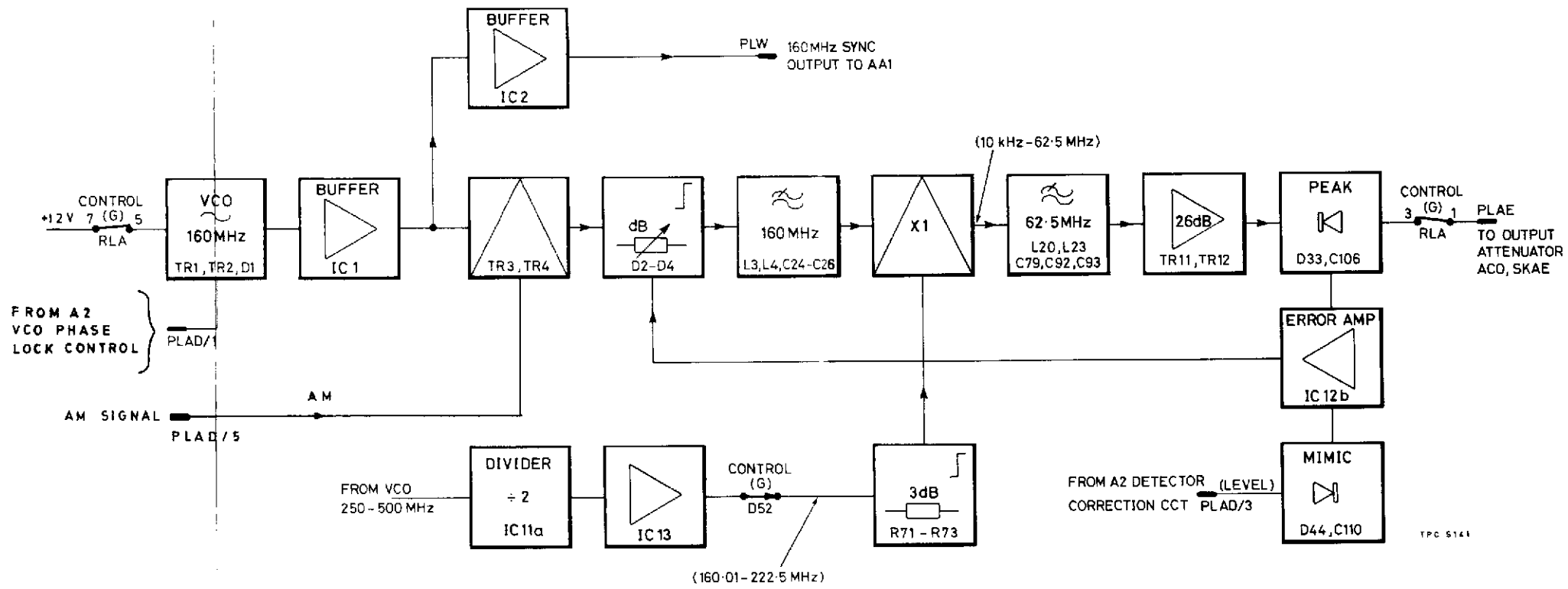


Fig. 10 BFO system & LF output stage (10 kHz - 62.5 MHz) simplified block diagram (AB1)

98. A mimic detector, D44 and C110 peak detects the combined level and a.m. signal arriving at PLAD pin 3. As the a.m. is added the r.f. level reference voltage at the junction of R105, R106 increases due to the action of D44. Since the reference and a.f. detected levels are summed at IC12 pin 6 the a.m. induced level error is cancelled out.

99. At low modulation frequencies the detector output will decay between envelope peaks at a rate depending on its time constant. In order to preserve the a.m. the reference voltage applied to the error amplifier must match the r.f. detector voltage exactly. If this is not accomplished IC12b error amplifier will produce a control signal that will tend to remove the a.m. from the r.f. signal. To make the reference behave in a similar manner as the a.f. detector voltage the mimic detector is set to have the same time constant as the r.f. detector.

100. The two detectors are of opposite polarity and C104 provides a long time constant to give a d.c. output from IC12b that is a measure of the error in carrier level irrespective of whether a.m. is in use or not. This is fed back to the current-controlled attenuator to set the level of signal at the mixer input such that the output level is correct. In common with the h.f. output amplifier, the signal is levelled as a voltage and R122 gives a source impedance of 50 Ω.

POWER SUPPLY/CONTROL (A0/A2)

Circuit diagram : Chap. 7, Figs. 2,4 & 5

101. The primary purpose of this board is to interface and control the various areas of the instrument that require access to the microprocessor via the internal instrument bus. There are three main areas on the board, analogue control, digital control and power supplies. These are described as follows:-

(1) Power supplies, four stabilized voltage lines are derived. These are +24 V, +12 V, +5 V and -12 V d.c. The +5 V rail chiefly supplies digital ICs. This is generated using discrete circuitry. The +12 V and -12 V rails supply a number of amplifiers and use monolithic 3-terminal regulators. A +24 V rail is used for low current purposes and is generated using a voltage doubler.

(2) Digital control section. Interrupts are controlled and routed to the microprocessor. A serial bus from the microprocessor is converted to an 8-bit parallel format which is then fed to latches on both A2 board and other boards. Address lines are also decoded on this board. The display drives on A1 board are supplied with a special format serial bus from A2 and data appearing on the 8-bit data bus can be converted back to serial data for transfer to the microprocessor.

(3) Analogue control. This area has several functions as listed below. Control data for each of the operations is routed via the 8 way bus:-

(1) Modulation signal a.l.c.
(2) Modulation depth or deviation control
(3) RF level control
(4) RF filter tuning
(5) Reverse power protection
(6) Attenuator drive
(7) Jitter correction drive

Power supplies

102. The a.c. mains supply range is set by two selector switches, SB and SC whose position is locked by a reversible locking plate. Supply transformer T1, and fuses FS1, FS2 are mounted on the rear panel assembly which can easily be hinged to provide access.

103. +5 V supply line. A0,T1, secondary 2 is used to supply rectifiers D1 and D2 via PLF pins 1,3 and 4. A2, IC3 controls the +5 V rail providing both short circuit current limiting and stable voltage regulation. A voltage reference diode, D10 provides a stable reference point on the resistor chain R12-R15 against which the sense point (junction of R19/R20/R112) is compared. R15 is adjusted for 5.1 V ±0.1 V.

104. If the sense voltage at R19/R20/R112 is greater than the reference voltage at the junction of R13/R14 IC3a output reduces and so does the drive to A2,TR1 base. R3 and R11 set the maximum permissible current limits for A2,TR1 collector and base respectively. A0,TR1 and A2,TR1 form a super beta pair with control of A2,TR1 base effectively setting the operating point of A0,TR1. The emitter of A0,TR1 is connected via R19 to the sense point so that reducing the current flowing into A2,TR1 base, current flowing through A0,TR1 also reduces. The voltage across the load will then fall to cancel the initial increase of sense voltage. This negative feedback system will equalize the voltage at the regulator output and at IC3a pin 3 to a nominal +5 V.

105. C49,C39 and R105 improve the transient response. Current limiting is achieved by monitoring the voltage drop across series resistor R19. Resistors R17 and R112 apply this voltage to IC3b. If due to excess current, the voltage at the junction of R16,R18 and R17 exceeds that on R112, then IC36 pin 7 will go negative, depriving A2,TR1 of base current by drawing it instead through R10 and D9. This will restrict the current flowing into the load.

106. In order to visualize the current limiting that occurs consider R16/R18 as a Thevenin equivalent (9.09 kΩ down to -1.09 V) and note that no current flows into IC3b pin 6. As the voltage at pin 5 falls, a lesser voltage at the top of R17 will be sufficient to bring the voltage of IC3b pin 6 up to equal that of IC3b pin 5. This implies a lower voltage across R19, i.e. the overall regulator current limit goes down as the output voltage goes down. This reduces short circuit dissipation in A0,TR1. However to provide assistance when fault finding, it is preferable to have some current flowing even under abnormal load conditions. The short circuit current is therefore deliberately not equal to zero.

107. +12 V supply line. A0,T1 secondary 1 winding is used to supply the bi-phase rectifier D3 which in turn charges C2. A0,IC1 and resistor chain A2, R4-R6 provide a +12 V regulated output with short circuit current limiting and over temperature protection. The voltage at PLH pin 5 is approximately 1.3 V below that at PLH pins 6 and 7 and the regulator A0,IC1 compares the voltage sensed at pins 5 and 7 with an internal bandgap reference. Current then flows out from the regulator via PLH pin 6 until the voltages equalize. PLH pin 7 receives a separate sensing signal from the regulator to improve the load regulation. D5 protects A0,IC1 from positive voltages on PLH pin 6 when PLH pin 4 voltage is low. C9 improves the ripple rejection.

108. -12 V supply line. Voltage in this circuit is generated in an identical manner to the +12 V supply except that the components are mounted on A2 board. One additional component, R108 is fitted to dissipate some of the heat generated and allow a smaller heatsink clip to be fitted to A2,IC1.

109. +24 V supply line & voltage doubler circuit is used to obtain this low current supply rail which is obtained via A0,T1 secondary 1 winding. All the components of the doubler circuit are mounted on A2 board. Consider the charge on C3; when the voltage at PLF pin 7 falls below zero C3 is charged through the lower left hand diode of bridge D4.

110. When the positive phase of A0,T1 begins, the positive charge on C3 will start to charge C6 through the upper left hand diode of bridge D4. If little current is drawn the charge on C6 will remain and eventually the voltage across it will build up to the peak output from A0,T1 and in addition the peak voltage developed across C3 i.e. approximately twice the peak output of A0,T1. C4 charges C6 during the negative cycles of A0,T1.

111. IC2 regulator is similar in its operation to A0,IC1 with resistor chain R7-R9, R8 providing the means of adjustment to +24 V ±0.25 V.

Digital control section

112. The circuit shown in Fig. 12 below illustrates how the microprocessor communicates with all the instrument latches, other than those on the synthesizer board. It does this over a serial bus which is converted to, and from, parallel data.

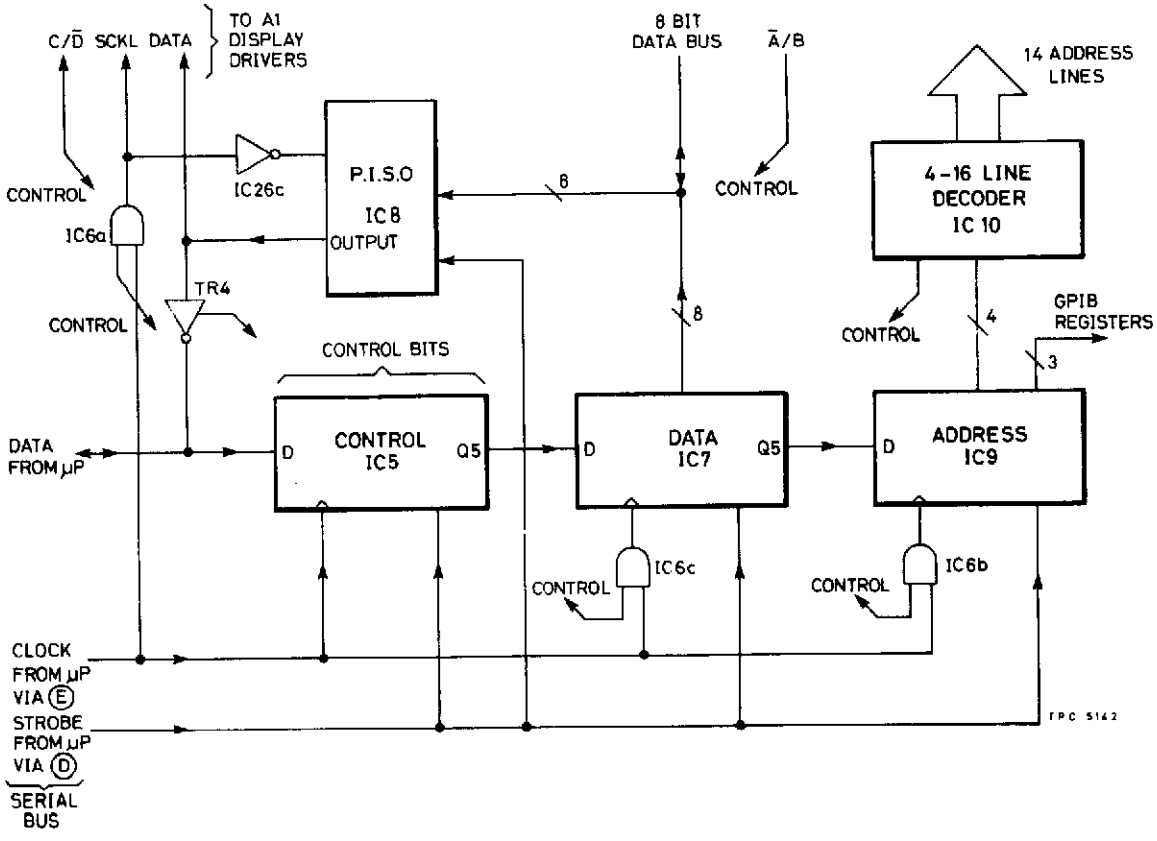


Fig. 12 Data conversion, simplified block diagram (A2)

113. Serial-parallel conversion, serial data is initially fed to IC5, pin 2 DATA input, shift register and is clocked in on the positive edge of the CLOCK input at IC5 pin 3. After eight bits have been entered, IC5 output Qs begins to change state; IC5 at this point acts like a delay unit eight clock cycles long i.e. data entered on the D input via IC5 pin 2 appears eight cycles later at Qs. It is also possible to transfer data that is clocking through on to the outputs Q1 - Q8. This is done by taking the STROBE line to logic 'high'. IC7 and IC9 are identical to IC5 in operation.

114. Since the clock inputs of IC7 and IC9 are gated (using IC6b and c) to IC5 outputs Q1 and Q2 respectively, IC5 must be loaded with the appropriate control byte before the data and address lines can be set. Having sent the first byte (containing data which will be discussed later), three more bytes need to be clocked through to load IC7 and IC9. The first will go direct to IC9, the second to IC7 and the last to IC5.

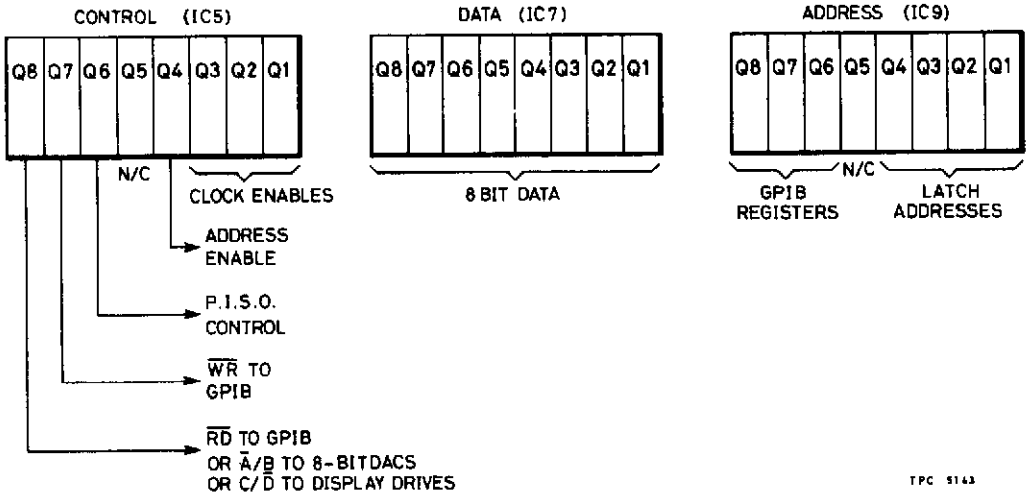


Fig. 13 Serial data string (A2)

115. Information loaded in the form shown in Fig. 13 is used in one of two formats. It will be used directly, as eight bits of parallel data everywhere except for the display driving. Thus data is set onto the bus and after leaving time to settle, IC10 output will be asserted 'low' temporarily. This will act as a strobe line. Since the digital-to-analogue converters (DACs) IC19, IC20, IC24 and IC27 are dual devices an additional decoding line is required. IC5, Q8 serves this purpose. It is also used in conjunction with Q7 to control the function of the GPIB if this optional accessory is in use.

116. If display data is required it has to be converted back into serial form before being sent to A1 display drivers, IC1 and IC2. However a variety of command data is required when the display is initially set at switch on and the differentiation is made by taking IC5, Q8 'high' instead of 'low'. As with the parallel mode, one of IC10 address decoders outputs will be taken 'low'. Data will be accepted on the returning positive edge.

117. Parallel to serial conversion. To change from parallel to serial format an 8-bit shift register, which may be pre-loaded, is used (IC8). Data present on inputs D0 - D7 is clocked out on Q8 and either sent to the display, in which case TR3 is switched on (Q6 of IC5 held 'low'), or sent back to the microprocessor. In the latter instance IC5,Q6 is held 'high' and TR4 acts as an inverter. C17,R24 and IC4 act as a monostable with an output duration of approximately 10 µs. This is triggered on a negative-going edge of the STROBE line. When the STROBE line is asserted 'low', parallel data is forced into IC8. This may then be clocked out by taking IC5, Q3 'high'. The use of a single clock ensures that the clock edges and the data are synchronized.

118. Interrupts. The microprocessor will normally be executing a 'zero task' whilst the instrument provides the output signal requested. If a change is required it must first be interrupted and then be made to respond according to the new information presented. The interrupts may be from any of the following four sources:

- GPIB
- Keyboard
- Reverse power protection system
- Modulation signal automatic levelling loop, i.e. signal too high or too low.

119. GPIB interrupt (High priority). IC4e, pin 3 will be asserted 'high' causing a negative-going edge to be sent to IC12d pin 11 and asserting IC13 pin 12 'low'. IC12d pin 13 will normally be at logic 'high' and IC12d NAND gate will function as an inverter causing a positive edge output to occur at the output on pin 11. This is then fed as the INTERRUPT line via PLL pin 13 to AA2 microprocessor. R25 prevents spurious interrupts if the GPIB is not connected. The microprocessor will react by addressing IC13 latch and reading D3 and D4 outputs to determine whether it is GPIB or keyboard requesting the interrupt. The microprocessor will then execute the necessary tasks to accept incoming data.

120. Keyboard interrupt (High priority), action here is the same as described above, IC6d pin 12 goes 'low', IC6d pin 11 also goes 'low' creating a positive edge on IC12d pin 11.

121. Reverse power protection system interrupt, relay AC1,RLF is normally energized when the instrument is switched on. Should there be an accidental application of reverse power the AC1,RLF will trip. A2,TR16 is turned off and IC12c pin 8 will go 'low'. IC12c pin will be 'high' therefore asserting IC12c pin 10 'high'. This will cause IC4f pin 4 to go 'low' causing a positive edge on IC12d pin 11. Pin 12 is held 'high' and a positive edge INTERRUPT pulse will again be created on IC12d pin 11 and routed to the microprocessor via PLL pin 13. To monitor keyboard interrupts (those required to reset the RPP) the outputs of IC13 are scanned. If a change is detected the normal keyboard reading sequence will occur but only RPP will have any effect. GPIB interrupts are also dealt with using the scanning process.

122. Modulation signal automatic levelling loop (a.l.c) interrupt, if the modulation signal applied is of a level that takes the control system outside preset limits (0 V and -6 V on IC15b pin 8) an interrupt will be caused. If the modulation level is insufficient, IC12a pin 1 will go 'low' and pin 3 'high'. IC12b pin 6 will normally be set 'high' thus pin 4 will go 'low'. IC12c pin 10 is then set 'high', IC4f pin 4 is sent 'low' and as before a positive edge on IC12d pin 11 INTERRUPT line is created. A similar action occurs if the modulation signal is excessive. This is the only interrupt that can be masked and this is carried out by setting IC11,Q3 'low'. If an interrupt from this system is read the microprocessor will periodically assert IC11,Q3 'high' and check to see if the modulation signal is within the specified limits.

Analogue control

123. Modulation signal a.l.c., this system is always in operation when the instrument is selected to INT MOD but can be selected in or out with the front panel MOD ALC key when in EXT MODulation mode. MOD ALC on is indicated by an l.e.d. adjacent to the key. The internal modulation signal is routed through RLA by taking IC11 Q0 'high'. R29 provides an approximate 600 Ω source impedance for the MOD IN/OUT front panel socket SKA.

124. IC15 is configured as a non-inverting amplifier with resistors R113 (adjust EXT MOD), R38, R35-R37 providing a feedback potential divider chain. TR6 is switched on via IC11 Q2 if MOD ALC is not required, this also switches TR7 off to give a fixed gain of nominally 3.54 from the circuit. If MOD ALC is selected TR7 then provides the mechanism for varying the gain of the stage by using it as an approximation to a voltage controlled resistor.

125. D14,C25 peak detect the output signal which is used as an offset against a negative voltage produced by R44,R45 and D15. Both voltages are summed at IC15 pin 9 and if the result is not zero then the output of IC15, pin 8 will integrate up or down charging C26. If IC15 pin 8 output were to increase (due to a low level signal at IC15 pin 7), then TR7 gate would also increase via R40 to turn on TR7 (R39,C24 improve the control/signal isolation).

126. When TR7 turns on its resistance between drain and source reduces and the gain of the stage increases. The output of the amplifier then goes up by a corresponding amount to give the required increase in output voltage. D16 improves speed by preventing C16 charging beyond +0.6 V. When the gate of TR7 is at 0 V, TR7 will be fully on - normal control is usually -3 or -4 V.

127. TR7's control voltage is monitored by IC18a and IC18b. If the level goes above 0 V IC18a's output switches low causing a 'LEVEL LO' interrupt. If the level goes below -6 V then IC18b output decreases and a 'LEVEL HI' interrupt is generated. It will simultaneously increase the signal level required for levelling at IC15a, pin 7. This hysteresis prevents multiple interrupts caused by a low frequency input signal whose level may be at the point of being just too high.

128. Modulation depth/deviation control. Three forms of modulation are possible a.m., f.m., or .m. These are controlled by three dual, digital-to-analogue converters (DACs). Both absolute level and calibration data are entered using these digital-to-analogue converters.

Amplitude modulation above 62.5 MHz

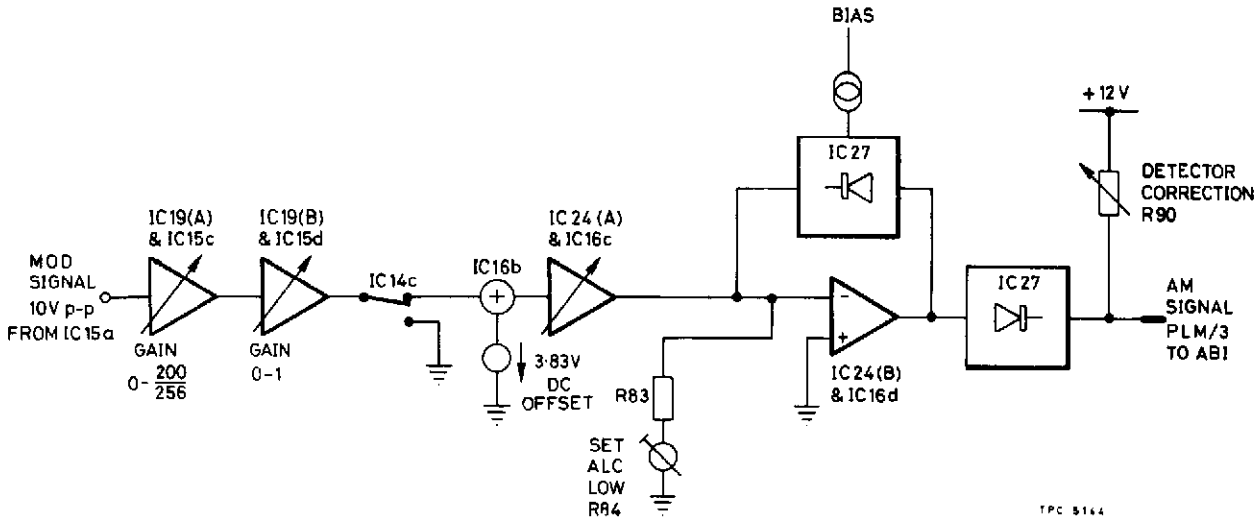


Fig. 14 AM signal path >62.5 MHz (A2)

129. The series path shown in Fig. 14 requires four sets of data to provide the correct signal. IC19(A) is loaded with a number proportional to the a.m. depth requested and IC19(B) has a.m. calibration data entered. IC24(A) will contain calibration data for the r.f. level and finally IC24(B) holds a number equal to the r.f. output voltage in mV (described in later paragraphs).

130. The a.m. depth is set by the ratio of modulation signal to d.c. level at IC24 input, pin 4. If the r.f. level is changed, the proportion of d.c. and modulation signal will stay constant and therefore so will the a.m. depth. AM depth of modulation up to 99.5% may be obtained for output levels up to 0 dBm but beyond this the combination of a.m. and power level will be restricted to ensure that peak powers of greater than +6 dBm are not requested.

131. If too great an a.m. depth is requested for a particular power level selected at that time, the power is reduced and a colon is flashed in the RF LEVEL display indicating the change and the new level selected.

132. The detector characteristic present on board AB1 is not an ideal one as can be seen in Fig. 15. It is therefore necessary to apply correction. At low r.f. levels (on AB1) the detected voltage rises with the square of the r.f. voltage. As the level increases above approximately 20 mV, however, the relationship becomes linear.

133. Consider Fig. 15. If we wish to obtain half the r.f. voltage VRFA, simply halving the reference voltage (and, due to loop action the detected voltage also, $\frac{VA}{2}$), will result in too low an r.f. level, (VRFB). For this reason the drive voltage must be greater at VB. IC27 and its associated circuit provides the necessary detector correction. The circuit is described in the following paragraph.

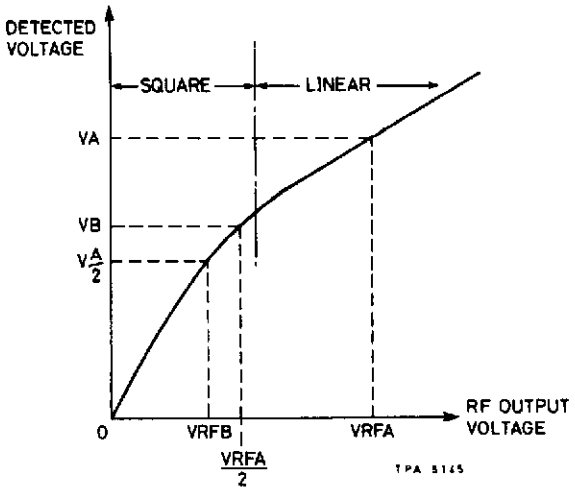


Fig. 15 RF detector law (A2)

134. Detector correction circuit. Two transistors in IC27 are used to predistort the signal that drives the envelope feedback system on the RF board, AB1. This only occurs at low voltage levels and the amount of shaping is determined by R93 (CORRECT DET) and the potential divider chain R91 and R92. A common drive signal appears on both transistor bases at pins 12 and 9 of IC27. The feedback signal comes from IC27 pin 13 via R85. R88 ensures that the left hand transistor is never turned off but merely provides temperature tracking of the diode characteristic of the right-hand transistor. The latter actually introduces the square law characteristic. This modified a.m. drive waveform is finally fed to the r.f. processing board AB1 via PLM pin 3.

Amplitude modulation below 62.5 MHz

135. To obtain the correct depth of modulation on signals below 62.5 MHz two drive signals are required. The first driver provides a fixed modulation at PLM, pin 5 via IC21b. The second driver ensures that the r.f. level reference that is ultimately applied to AB1 comparator is increased by an amount equal to the detector voltage increase due to the a.m. If this is not achieved there will be a shortfall in r.f. level.

136. Fig. 16 shows the signal path for the two a.m. drive signals. IC21b provides the drive for the fixed frequency modulator. The gain of this stage is such to allow the full 100% modulation. Depth is set by data entered into the digital-to-analogue converter IC19(A), and calibration data is entered via IC19(B). R111 prevents capacitive loading affecting IC21b.

137. The modulation signal is also fed via IC14c and IC16b through IC24 and uses the same signal path as signals above >62.5 MHz but in this case the square law transfer characteristic is no longer of any consequence.

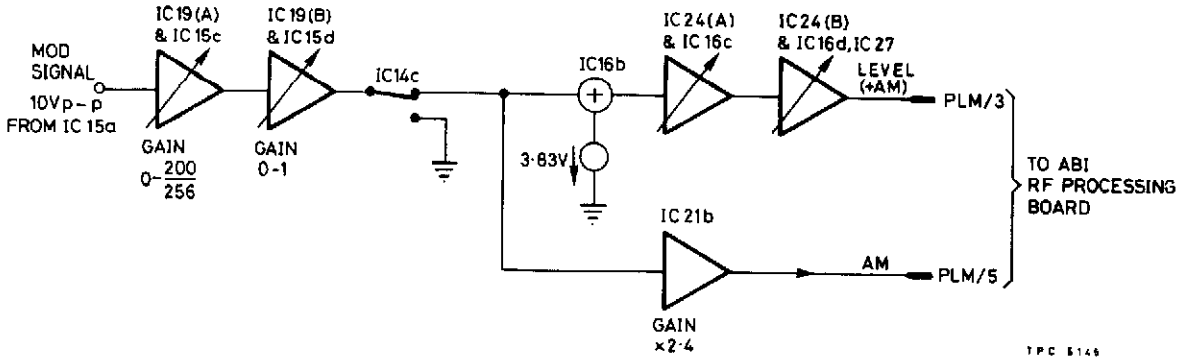


Fig. 16 AM signal path <62.5 MHz (A2)

Frequency modulation

138. In order to obtain the necessary low modulation frequency response on f.m. two signal paths are used. One path drives the v.c.o. tuning line whilst the other is used to modulate the phase of the reference signal used in the 250 - 500 MHz phase locked loop (p.l.l). If the second path was not included the action of the p.l.l. would be such that where the modulation frequency is below that of the loop bandwidth (200 Hz), it would be removed from the r.f. signal.

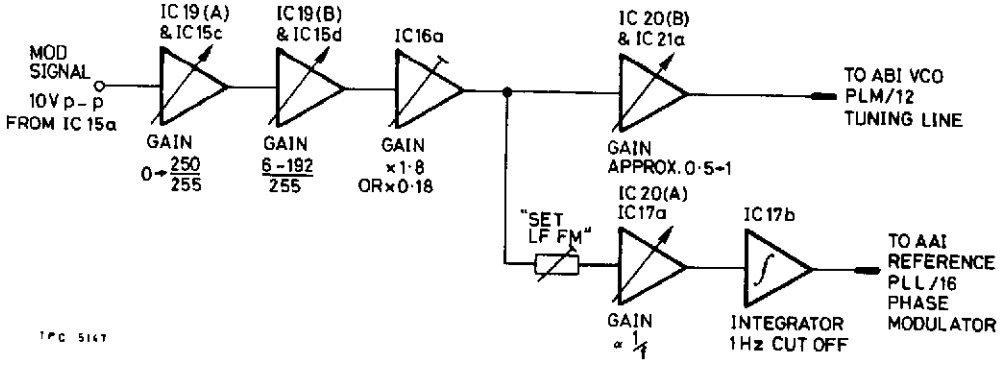


Fig. 17 Dual path f.m. drive (A2)

139. VCO tuning line drive. IC19 DAC changes the drive level according to the peak deviation requested. IC19(A) is loaded with a number proportional to that deviation whilst IC19(B) has a multiple of 6 which changes according to the carrier frequency selected and maximizes the resolution of IC19(A).

TABLE 1 DAC VALUES FOR VARIOUS FM DEVIATIONS (A2)

Deviation	Value in DAC
0 - 249	Deviation
250 - 499	Deviation ÷2
500 - 999	Deviation ÷5

140. Table 1 shows how a resolution of 0.4% of full-scale deviation is achieved. IC16a has a gain set by R50/R51 or R52/R53 dependent on the value of deviation selected. For values less than 10 kHz it is x 0.18 and for deviations between 10 - 100 kHz it is x 1.8. MOS switch IC14 effects the change of gain via two output lines from IC11, Q4 and Q5. Control data on these lines are shown in Table 2. Virtual earth switching ensures that the resistance of the switch when on has negligible effect on the gain of the stage. D22,D23, ensure no distortion occurs when a channel is not in use. R31 and R32 provide the correct bias level for IC14 switches.

TABLE 2 DECODING OF FM/ΦM FUNCTIONS (A2)

IC14 Q4	IC14 Q5	FUNCTION
0	0	FM 0 - 9.99 kHz
0	1	ΦM 0 - 9.99 rads
1	0	FM 10 - 99.9 kHz
1	1	Not used

141. IC20(B) is fed from IC16a and the non-inverting input on the associated IC21a, pin 3 is taken to ground on board AB1 via PLM, pin 2. This minimizes spurious modulation caused by induced voltages.

142. Reference phase modulator, low f.m. path. This second path drives a phase modulator on board AA1. To obtain an equivalent frequency modulation the modulation signal must be applied through an integrator. To consider why this is necessary, imagine the effect of a steady voltage being applied to the modulator. Without an integrator a steady phase error would be created. With the integrator in however an increasing phase error with respect to time will occur and this gives the required frequency shift.

143. To maintain the correct loop operation the modulation of both the v.c.o. and the reference phase signal must be identical therefore producing no error signal at the output of AA1 main synthesizer phase detector. To this end IC20(A) is loaded with data that is proportional to the frequency at which the 250-520 MHz synthesizer is operating. As the synthesized frequency increases, the ratio of deviation to synthesizer frequency reduces and a smaller phase change at the phase detector will cancel it out. The reduction of gain in IC20(A), due to its configuration, will track this requirement.

144. The 'SET LF FM' potentiometer R58 and resistors R57, R59 ensure that the above described correction can be attained. Correct setting of R58 will ensure a substantially flat frequency response from less than 10 Hz to well above 25 kHz.

145. IC17b with its associated circuit forms an integrator with a low frequency roll off at approximately 1 Hz. DC feedback is maintained through R71, R72, R62 and R64 and the integrating action is given by R63 and C33. The low frequency cut off is due to the input coupling capacitor C32 and feedback decoupling capacitor C40. The integrated signal is fed to AA1 via PLL pin 16. In order to optimize the response of low frequency square waves the overall amplitude response of IC17b circuit actually has a slight rise around 1 Hz before dropping off below this frequency at 12 dB/octave.

Phase modulation

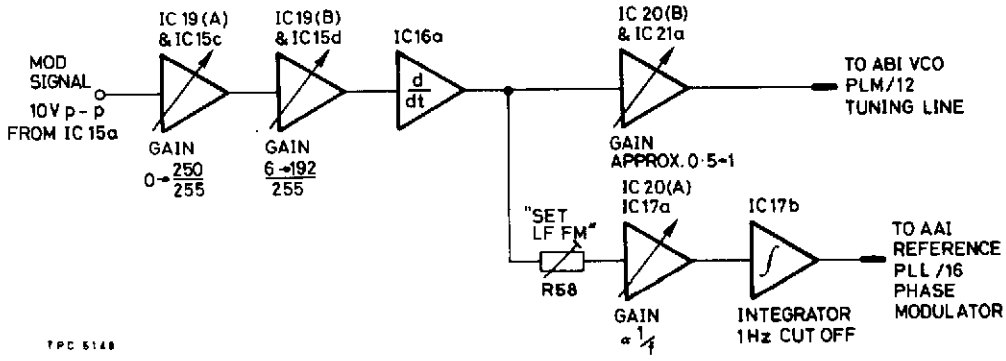


Fig. 18 Phase modulation signal path (A2)

146. Since this is 'angle' modulation, like f.m., the signal path is similar to that described in the frequency modulation paragraphs previously. The only difference being that IC16a is converted from a gain stage to a differentiator providing a 6 dB/octave pre-emphasis. R55, R56 and C29 are set for the main time constant whilst R54 restricts the gain at high frequencies to reduce noise in that area. R56 'SET ΦM' allows calibration of the system.

RF level control

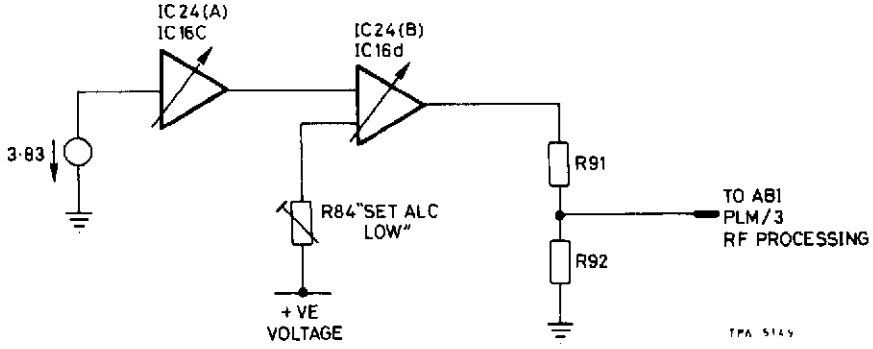


Fig. 19 Simplified r.f. level control signal path (A2)

147. This control circuit is used over the complete carrier frequency range. RF processing board AB1 requires a voltage that approximates to an offset plus a variable voltage that is dependent on the r.f. level requested. The square law consideration discussed in the a.m. modulation paragraphs is of little importance for simple level changes because the range is limited from -12 dBm to +6 dBm. The voltage at PLM pin 3 must correspond to approximately twice the actual peak r.f. level requested due to the 50 Ω source resistor on board AB1.

148. IC16b with R70 and R74 provide a constant voltage of -3.83 V. C52 decouples the reference line to ground. Data is entered into the digital-to-analogue converter, IC24 in one of two formats, for r.f. output levels below 256 mV r.m.s. a number equal to the output voltage in mV is sent to IC24(B) whilst a calibration value (which could be up to 127_{10}) is entered into IC24(A).

149. If the r.f. level requested is greater than 255 mV then the value in IC24(B) is half the level in mV and the calibration value is doubled as can be seen in the following table.

TABLE 3 RF LEVEL CALIBRATION DATA, IC24 (A2)

RF level	IC24(B)	IC24(A)
56 - 255 mV	56 - 255 mV	CAL DATA
256 - 446 mV	$\frac{256 - 446 \text{ mV}}{2}$	x 2 CAL DATA

150. R84 'SET ALC LOW' and R88 allow the required offset to be introduced. This is effected at the summing inverting input of IC16d. The d.c. level is then transferred to AB1 via the base emitter junction of the right-hand transistor of IC27, potential divider R91, R92 and PLM pin 3.

RF filter tuning

151. Two tracking filters are used on board AB1. One is a notch used to reduce the second harmonic component of the oscillator output; the other is a band-pass filter used to reduce unwanted components on the doubler output. The latter has no means of adjustment and so calibration data is entered into A2, IC23(B) to ensure that the band-pass filter operates at the correct frequency. The notch filter is then adjusted to reject the second harmonic of the oscillator output with the oscillator set to its lowest operating frequency (250 MHz). The tuning law of the band-pass filter and notch are sufficiently alike to allow the same tracking data to be used in both cases.

152. IC23, pin 18 is coupled to the -12 V line, this is inverted and then multiplied by IC17d. TR13 ensures that the maximum tuning range is available, allowing PLM, pin 15 to be taken to within 0.5 V of the +24 V rail. R80, R81 provide the correct bias for TR13 and R82 increases the gain of IC23(B) from x1 to approximately x2.

Reverse power protection switching and attenuator drive

153. IC22, IC18c and IC18d with their associated circuits control the operation of AC1 attenuator relays. Latch IC22 is fed with data dependent on the level of fixed attenuation required, details of which can be seen in Table 4.

TABLE 4 ATTENUATOR SWITCHING LOGIC (A2)

Attenuation	Q_0	Q_1	Q_2	Q_3	Q_4
0 dB	1	1	1	1	1
10	1	1	1	0	1
20	1	0	1	1	1
30	0	1	1	1	1
40	0	1	1	0	1
50	0	0	1	1	1
60	0	1	1	1	0
70	0	1	1	0	0
80	0	0	1	1	0
90	0	1	0	1	0
100	0	1	0	0	0
110	0	0	0	1	0
120	0	0	0	0	0

154. When the required selection is made the respective Q output line(s) are grounded and the associated transistor (TR8 - TR12) is turned on. Base current flows via the load resistors (R75 - R78) and diodes D17 - D21 protect

the transistors from the large negative-going inductive spikes created when the relays are turned off. Relay current flows via PLN pins 2 - 7. Thus if a particular pad is required current is supplied to that pad's relay.

155. IC18c and IC18d are comparators monitoring the voltage levels present on the attenuator. If PLN pin 9 voltage should exceed +0.04 V (when a voltage overload is applied to the RF OUTPUT socket) IC18c will switch its output to a high level. D24 and D26 then conduct and turn off TR16. This in turn will cause the RPP relay AC1, RLF to drop out and at the same time initiate an interrupt, RPP TRIPPED L, to the microprocessor. This would be in the form of a logic 'low' level applied to IC13, pin 6 via R104.

156. Similarly, if a negative voltage overload is applied to the RF OUTPUT socket this will cause PLN, pin 10 voltage to fall below -0.04 V. IC18d output will be set 'high' and again TR16 will be turned off via D15, D26 and R101. R103 ensures that the energy stored in the RPP relay is dissipated in the least time possible.

157. RPP reset, if either IC18c or IC18d output goes 'high', R100 pulls the comparison level of IC18d above 0 V. Since AC1 negative detector D2 will be unable to reach this level IC18d would remain at logic 'high' output even after the overload is removed. It is therefore necessary to apply an external reset. When the RPP is tripped the keyboard is disabled with the exception of the RF LEVEL key. The REV PWR annunciator will flash on the RF LEVEL display to indicate the presence of an overload. No further keyboard operation can be made until the RPP is reset by pressing the RF LEVEL key.

158. On pressing the key IC22,Q5 output will be set from 'low' to the 'high' state, the positive edge is transferred via C38, to the junction of R96, R97. If the magnitude of the detected voltage is less than 40 mV IC18d output will change from 'high' to a 'low' state and TR16 will again be turned on. AC1, RLF energizes and normal operation is resumed. If the overload is still present IC18d output will remain 'high' and the RPP will not reset.

Jitter correction drive

159. In order to reduce phase jitter of the carrier frequency which is introduced by the fractional N technique, an offsetting phase error is required. A circuit on the Synthesizer board AA1 generates this but a reference voltage, inversely proportional to the synthesized frequency is required. IC23(A) and its associated circuit provide this function.

160. R66, R68 and R67, CORRECT JITTER, provide an adjustable reference that feeds digital-to-analogue converter IC23(A). IC17c and IC23A are configured to give a gain that is inversely proportional to the value of data entered into the digital-to-analogue converter. The eight most significant bits of the synthesizer frequency are entered into the digital-to-analogue converter and thus the output of IC17c pin 8 will be a voltage that goes down as synthesizer frequency goes up. It is sent to AA1 via PLL pin 1 as the JITTER CORRECTION REF.

DISPLAY AND KEYBOARD (A1)

Circuit diagram : Chap. 7, Fig. 3

161. The keyboard facilitates instrument operation by interrupting the microprocessor (through a priority tree) which runs an interrogation of the keyboard matrix to locate the switch selection. The microprocessor then runs

a new task appropriate to the key(s) pressed. Information giving the current state of the instrument is continually displayed and includes frequency, r.f. level and modulation.

162. Data is displayed on a combined two phase multiplexed liquid crystal display (l.c.d.). Eight light emitting diodes (l.e.d's) are also used to indicate the function currently selected. Two specialized integrated circuits convert serially transmitted information into the waveforms required to drive the l.c.d. Drive information for the l.e.d's is provided by a single latch.

Keyboard operation

163. Switches are arranged in a six-by-six matrix and are connected in rows to IC3 data latch. Initially the rows are set to a logic 'low' level. The columns of the matrix are connected to R9 pull-up resistors, which initially set all the columns to logic 'high' level. One of the resistors, R9(h) is a pull-up for D9-D14 six input gate. This gives an OR function using negative logic convention.

164. The columns drive both the six input gate and IC5 data latch. IC5 controls the data bus via SKK pins 5-8 and 13-16. When a key is pressed a connection will be made from the column that the key is in to the row that the key is in. This causes the column to be asserted 'low' because all of IC3 Q outputs are held logic 'low'. A connection from the diode gate is also made to the microprocessor via SKK pin 11. This line KEYBOARD INT L when asserted 'low' causes the microprocessor to commence running a new task. This will in turn assert all but one of IC3 Q outputs logic 'high'; each output in turn then reverts to logic 'low' commencing with Q0. As this occurs the columns are monitored by IC5.

165. If the 6-bit word being output by the matrix is not all '1's then the word is digitally rotated to find which column has a logic 'low' on it. The combination of row and column data thus obtained is used to address a look up table which gives the code of the key pressed.

LED display

166. The eight diodes D1-D8 provide 'state' information relating to the function switches. This allows unambiguous keyboard operation. IC4 is an eight-bit data latch that drives the l.e.d's through R10-R13 current limiting resistors. Only four resistors are required for the eight l.e.d's because only one diode of D4-D8 will be lit at any one time. Data is placed on the bus and then chip select CS4 is taken to logic 'high' momentarily. All IC4 outputs are continuously enabled and thus any of the inputs, D0-D7 which were 'high' when CS4 went 'high' will give a logic 'high' output on Q_0-Q_7. The nominal diode current taken by a diode when operating is approximately 15 mA.

LCD display

167. IC1 and IC2 are the l.c.d. controllers which accept complex strings of serial information on pin 9 via the Serial Input (SI) line. They are able to store this and use it to control which of the 128 display segments are turned on. Chip select lines CS1 and CS2 determine which IC is to receive data and the Command/Data (C/D) line determines the way that the data is processed.

168. Serial Clock Low (SCK L) line is clocked from A2 board via SKK pin 2. The positive-going edge of SCK L cues the selected IC so that the serial input, SI

line can be read. The display has two phases of backplane drive to enable two segments to be connected with a single drive point. This halves the number of drive points required.

169. R8 sets the internal clock frequency for both IC1 and IC2 and is divided by 2^{11} which actually results in a backplane frequency of approx. 40 Hz for display driving. The common connection between pin 2 of IC1 and IC2 ensures that both are synchronized. Reset lines are coupled together and then connected via SKK, pin 18 to a latch on A2 board. At switch on and at any time the +5 V rail falls below a preset value the reset line will be asserted logic 'low' and all data will be cleared from IC1 and IC2. It is necessary to hold this line 'low' until the correct supply voltage is available to ensure synchronization of the display backplane drives.

170. The display drive waveform is switched between three voltage levels provided by TR1 and R1-R7. These are nominally (i) $VLCD_3$ (+0.9 V) (ii) VDD (+5 V) (iii) $VLCD_1$ (+3 V), midway between VDD and $VLCD_3$. The voltage on TR1 collector varies with temperature to match changes that occur in the l.c.d. fluid.

Two phase multiplexing

171. Liquid crystal displays are passive unlike l.e.d. active displays, which convert energy into light. In the 2022 multiplexed l.c.d's use a feature of the fluid in the device to provide the display required. Changes in the polarization of light passing through it do not occur until a certain r.m.s. voltage is reached. Once this level has been exceeded the segments to which the signal is being applied appear dark.

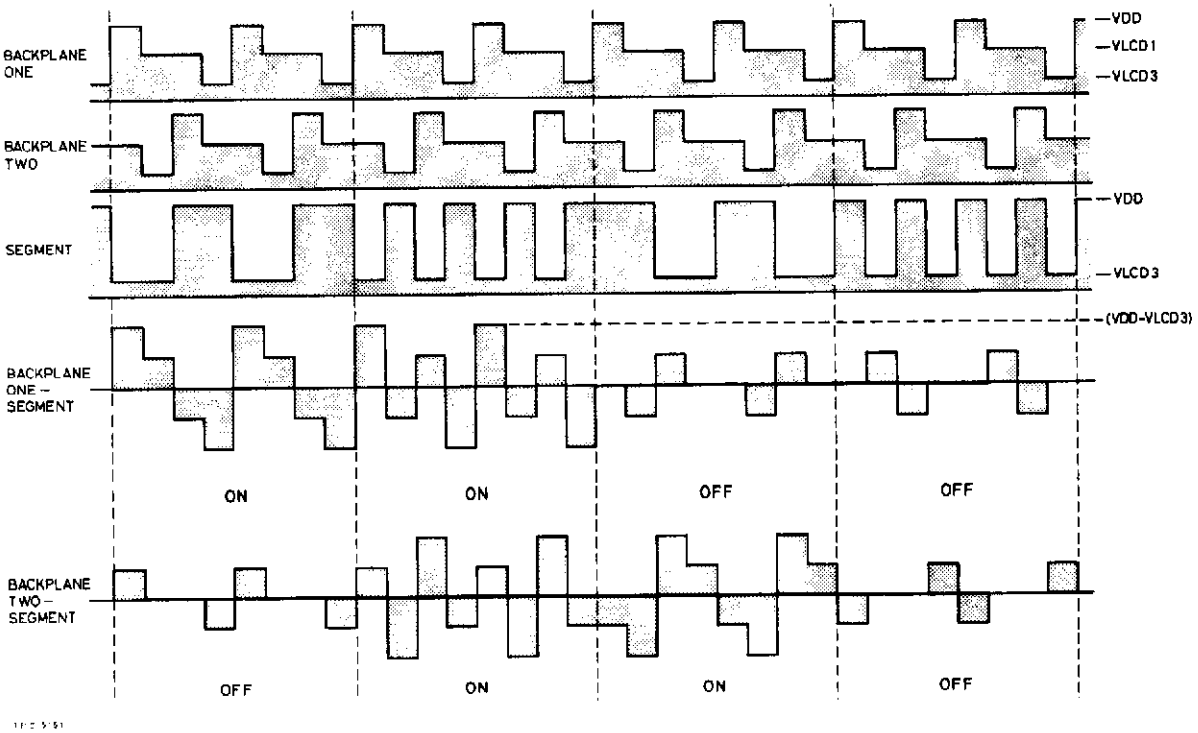


Fig. 20 Typical waveforms, l.c.d. drive waveforms (A1)

172. Fig. 20 shows typical waveforms generated at IC1 and IC2. There is a $\sqrt{5}$:1 difference in the r.m.s. voltage between segment and backplane plates depending on whether the segment is on or off. The backplanes remain as shown with a 180^0 phase difference whilst the segment drive takes up one of four possible forms to produce the four states required.

10 dB STEP OUTPUT ATTENUATOR (AC0/A2)

Circuit diagram : Chap. 7, Figs. 5 & 9

173. Instructions to operate the attenuator pads are initiated by means of the keyboard and are then processed by the microprocessor via data lines D0-D4. A2 board IC22 receives a logic 'low' instruction to cause one (or more) of five control transistors TR8-TR12 to turn on. This in turn completes the current path for one or more selected relays on board AC1 via PLN pins 2-7. Relays RLA-RLE are normally de-energized until the current path for the attenuator pad(s) relay is completed. When this occurs current flows through the respective attenuator pad(s) relay and the contacts then make to bring the pad(s) into circuit.

174. Diodes D17-D21 on A2 board act as clamps to protect the open collector drivers TR8-TR12 from inductive spikes. When a relay is de-energized the stored magnetic field causes a large negative-going voltage spike on the control line which is clamped by the diodes. Adjustment to the attenuator pads are made by means of screws in the lid. Frequency response is optimized by the adjustment of small flags which are moved by these screws. Each pad is set up separately and requires the use of specialist measuring facilities. It is therefore recommended that this is carried out by the nearest Marconi Instruments Agent or Service Division.

175. Each attenuator pad consists of 3 precision resistors that provide attenuation of 10 dB, 20 dB or 30 dB. Logic selection for each of the 10 dB steps from 0 to 120 dB is shown in Table 5.

TABLE 5 ATTENUATOR LOGIC (AC0/A2)

dB Attenuation			0	10	20	30	40	50	60	70	80	90	100	110	120
Pads in circuit	A	30 dB				X	X	X	X	X	X	X	X	X	X
	B	20 dB			X			X			X			X	X
	C	30 dB										X	X	X	X
	D	10 dB		X			X			X			X		X
	E	30 dB							X	X	X	X	X	X	X

X = Relay energized

Reverse Power Protection (AC0/A2)

176. Resistors R16 and R17 form a high impedance r.f. signal divider at the output of the attenuator which is used to sense the r.f. present at the output of the attenuator. Diodes D1 and D2 peak detect the signal level onto C14 and C16. The resulting d.c. is connected for use in the r.p.p. system. If the signal level exceeds a preset limit relay RLF de-energizes and sets the contacts to open circuit the output to SKAF, thus protecting the attenuator from excessive power dissipation.

177. Decoupling capacitors C1-C12 and inductors L1-L8 reduce coupling of r.f. voltages present inside the attenuator onto drive lines outside the box.

GPIB ADAPTER MODULE (AD0)

Circuit diagram : Chap. 7, Fig. 10

178. This optional module, when fitted to the rear panel, allows direct connection to a GPIB controller and provides full talker/listener facilities to IEEE 488 specifications.

179. GPIB talker/listener integrated circuit IC2, is connected to A2 board via SKP providing both talker and listener capabilities, details of these are given in Chapter 3 of the Operating Manual. IC2 contains the gating registers and control circuit needed to interface between the GPIB and the instrument's 8-bit bus. Fig. 21 shows the basic structure of the device. In its most elementary form data is entered into one of the internal registers and then transferred to the GPIB or instrument bus depending on whether a talk or listen mode is chosen. Further information on the general features and applications of the GPIB system can be obtained from the separate GPIB manual (see Vol. 1, Optional accessories).

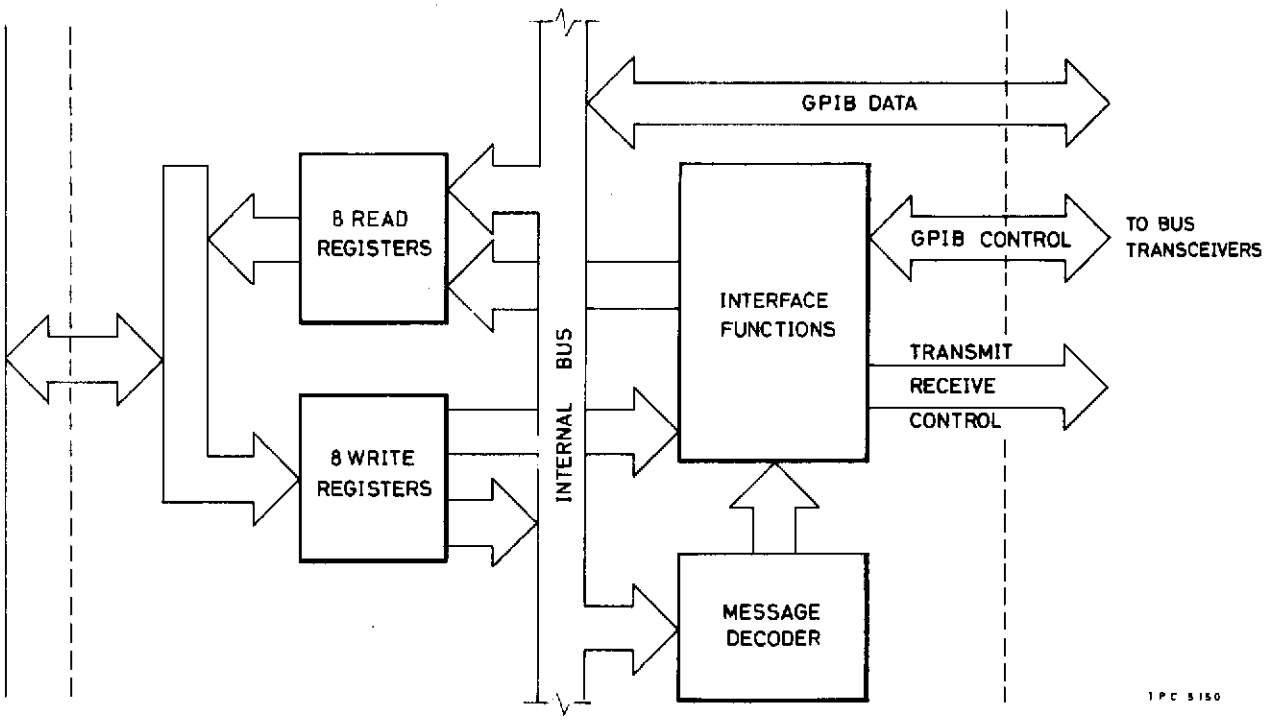


Fig. 21 Internal structure of GPIB talker/listener integrated circuit, IC2 (AD0)

180. IC1, R1 and C8 operate as an independent clock whose frequency (between 1 and 2 MHz) is used to generate a delay of approximately 2 µs allowing the bus to settle after sending data. IC1a is a Schmitt triggered input inverter with R1 and C8 providing positive feedback to complete the oscillatory circuit. IC1b buffers the clock signal, which is fed directly to IC2, GPIB chip.

181. Sixteen lines are buffered by IC3-IC6, these act as transceivers and are used to translate the negative true logic and act as drivers. Data lines, DAV, NDAC, NRFD and EOI lines have bi-directional buffers. The remaining lines with the exception of the SRQ line are receivers. IC1e,f provides the logic "low" level for the receive instruction T/R to IC4 pins 7 and 9; or the talker "high" level for IC4,IC5 and IC6 and also provides additional buffering for the three ICs in line. IC2 pin 2 controls the mode of the EOI line.

SECOND FUNCTION OPERATIONS

182. Second function operations provide the means of controlling various secondary features and calibrations within the instrument. There are three levels of operation, two of which require unlocking in order to gain access. Each level of operation and method of access is described below.

183. **Normal operation**

Second functions	"0"	Unlock	These functions are unprotected and may be accessed directly:- Press 2ND FUNCT followed by the numeral required.
	"1"	Status information	
	"2"	GPIB address setting	
	"3"	Manual latch setting	
	"4"	SRQ mask setting	
	"5"	Read identity string	
	"6"	Front panel "Test display"	
	"7"	Reserved for future use	
	"8"	Reserved for future use	
	"9"	Read elapsed time since last reset	

184. **First level operation**

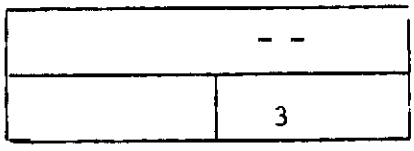
Second functions	"10"	Record external freq. std. choice	These functions have first degree protection and are accessed by the following procedure:- Press 2ND FUNCT 0, then the ↓ (decrement) and MOD ALC keys simultaneously, holding both these down until a "1" appears in the Frequency display. Follow this by again pressing 2ND FUNCT, and the numerals required.
	"11"	Read identity string	
	"12"	Write user-definable string (GPIB only)	
	"13"	Read user-definable string (GPIB only)	
	"14"	Set r.f. level units setting	
	"15"	Set r.f. level offsets	
	"16"	Recall STORE 10 at switch on	
	"17"	Reserved for future use	
	"18"	Reserved for future use	

185. **Second level operation**

Second functions	"190"	Set identity string	These functions have second degree protection and are accessed by the following procedure:- 2ND FUNC 0, then in the following order ↓ (decrement), MOD ALC, 4 and kHz keys, holding down all four until a "2" appears in the Frequency display. Follow this by again pressing 2ND FUNCT and the numerals required.
	"191"	FM tracking calibration	
	"192"	RF level calibration	
	"193"	Voltage tuned filter (VTF) calibration	
	"194"	AM calibration	
	"195"	Calibration and storage of amended EAROM checksum	
	"196"	Protection of store settings	
	"197"	Display blanking of recalled stores	
	"198"	Read total instrument operating time	
	"199"	Reset of second function 9 elapsed time.	

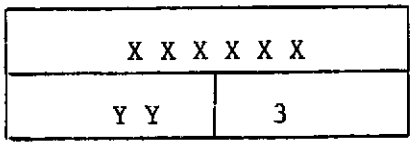
186. Second function '3' Manual latch setting. Second functions that are used in normal operation of the instrument are described in the Operating Manual Vol. 1. Second function 3 Manual latch setting however is used only in maintenance applications and is therefore described here. This facility allows the operator to direct a 6 or 8 bit binary instruction to any of the instrument's internal latches or registers for testing and fault finding. The latch is accessed by first selecting 2ND FUNCT 3 mode then keying in the address number, 00 to 35. Latch address numbers are identified in both Chap. 7 Servicing diagrams and Chap. 5 Maintenance.

187. Selection of second function 3 results in the following display:-



The instrument now awaits entry of the latch number which will be displayed in the carrier frequency window until selection is completed. When this occurs the display will change to one of two formats depending on whether a 6-bit or an 8-bit latch has been addressed.

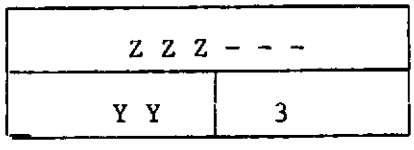
188. 6-bit latches, when the address latch number has been entered the display will change and the current value of data normally applied to the latch is presented in binary notation as shown in the example below:-



Where XXXXXX = binary data
YY = latch number
3 = second function selection

189. Data can now be entered in binary (6 digits 000000 to 111111), with data being shifted in, most significant bit first. When data is satisfactorily set press the STORE key to terminate the entry; the decimal points will flash briefly to indicate that the data has been sent.

190. 8-bit latches, selection of an 8-bit latch or register will result in an identical initial display as that shown for a 6-bit latch selection. However, when address selection is complete data is displayed not in binary but decimal notation in the following manner:-



Where ZZZ = present decimal data
--- = new data entry point
YY = latch number
3 = second function selection

SECOND FUNCTION OPERATIONS

182. Second function operations provide the means of controlling various secondary features and calibrations within the instrument. There are three levels of operation, two of which require unlocking in order to gain access. Each level of operation and method of access is described below.

183. Normal operation

Second functions	"0"	Unlock	These functions are unprotected and may be accessed directly:- Press 2ND FUNCT followed by the numeral required.
	"1"	Status information	
	"2"	GPIB address setting	
	"3"	Manual latch setting	
	"4"	SRQ mask setting	
	"5"	Read identity string	
	"6"	Front panel "Test display"	
	"7"	Reserved for future use	
	"8"	Reserved for future use	
	"9"	Read elapsed time since last reset	

184. First level operation

Second functions	"10"	Record external freq. std. choice	These functions have first degree protection and are accessed by the following procedure:- Press 2ND FUNCT 0, then the ↓ (decrement) and MOD ALC keys simultaneously, holding both these down until a "1" appears in the Frequency display. Follow this by again pressing 2ND FUNCT, and the numerals required.
	"11"	Read identity string	
	"12"	Write user-definable string (GPIB only)	
	"13"	Read user-definable string (GPIB only)	
	"14"	Set r.f. level units setting	
	"15"	Set r.f. level offsets	
	"16"	Recall STORE 10 at switch on	
	"17"	Reserved for future use	
	"18"	Reserved for future use	

185. Second level operation

Second functions	"190"	Set identity string	These functions have second degree protection and access to Second level operation is restricted to authorized calibration units only. Interference with these second functions could invalidate the instrument's calibration.
	"191"	FM tracking calibration	
	"192"	RF level calibration	
	"193"	Voltage tuned filter (VTF) calibration	
	"194"	AM calibration	
	"195"	Calibration and storage of amended EAROM checksum	
	"196"	Protection of store settings	
	"197"	Display blanking of recalled stores	
	"198"	Read total instrument operating time	
	"199"	Reset of second function 9 elapsed time.	

186. Second function '3' Manual latch setting. Second functions that are used in normal operation of the instrument are described in the Operating Manual Vol. 1. Second function 3 Manual latch setting however is used only in maintenance applications and is therefore described here. This facility allows the operator to direct a 6 or 8 bit binary instruction to any of the instrument's internal latches or registers for testing and fault finding. The latch is accessed by first selecting 2ND FUNCT 3 mode then keying in the address number, 00 to 35. Latch address numbers are identified in both Chap. 7 Servicing diagrams and Chap. 5 Maintenance.

187. Selection of second function 3 results in the following display:-

	- -
	3

The instrument now awaits entry of the latch number which will be displayed in the carrier frequency window until selection is completed. When this occurs the display will change to one of two formats depending on whether a 6-bit or an 8-bit latch has been addressed.

188. 6-bit latches, when the address latch number has been entered the display will change and the current value of data normally applied to the latch is presented in binary notation as shown in the example below:-

X X X X X X	
Y Y	3

Where XXXXXX = binary data
YY = latch number
3 = second function selection

189. Data can now be entered in binary (6 digits 000000 to 111111), with data being shifted in, most significant bit first. When data is satisfactorily set press the STORE key to terminate the entry; the decimal points will flash briefly to indicate that the data has been sent.

190. 8-bit latches, selection of an 8-bit latch or register will result in an identical initial display as that shown for a 6-bit latch selection. However, when address selection is complete data is displayed not in binary but decimal notation in the following manner:-

Z Z Z - - -	
Y Y	3

Where ZZZ = present decimal data
--- = new data entry point
YY = latch number
3 = second function selection

Decimal data entered will shift in most significant digit first. On completion press STORE key, when the data on the right of the display will be sent to the latch. This is indicated by the instrument copying the new entered data into the left side of the frequency window and replacing the right side with " --- ", ready for a further entry.

191. Any new data sent to a 6-bit or 8-bit latch will remain valid until the manual latch addressing mode is terminated by pressing one of the main function keys. At this time the latch data will be restored to its normal status.

192. Second function ´190´ Set identity string, this facility is second degree protected and is only normally required to initialize the instrument. The identity string shows the instrument type number and serial number. This information can be read via the GPIB. A typical display is described in the Operating Manual Vol. 1 Second function 5 Read identity string. Instrument type number and software issue number is shown first e.g. 52022-900, then the software issue number e.g. 004. This cannot be changed via the keyboard as it is built into the software. Pressing the ´.´ decimal point key then allows the second half of the string containing the serial number of the instrument to be entered.

193. Entering digits first clears the display and then rotates the numbers in from the right-hand side of the frequency display. When setting the first half of the string the most significant digit will be entered but will rotate off the end of the display. Press STORE to terminate this entry. Press ´.´ (decimal point) to display the second part of the string and key in the nine digits required to enter the serial number, in this event the two most significant digits will not be displayed. Again press the STORE key to terminate the entry. In each case pressing the STORE key will show the new data in the normal display format.

194. Second function ´191´ FM tracking calibration. The f.m. tracking calibration data consists of two tables of calibration points. The first, which covers the frequency range 250.0000 MHz to 352.9999 MHz, has 25 calibration points spaced 4.12 MHz apart, with the exception of point 24 which is 100 Hz less than 4.12 MHz (4.1199 MHz) to avoid overlapping with the higher table. The second table covers frequencies from 353.0000 MHz to 499.9999 MHz and also has 25 points, each 5.88 MHz apart except for the 25th point. This is again 100 Hz less (5.8799 MHz), to avoid overlapping with point 24. Details of the calibration procedure are given in Chap. 5 Maintenance.

195. Second function ´192´ RF level calibration. The output level is calibrated at 11 selected reference points, each point is numbered from 00 to 10 with the selected point displayed in the modulation window. Point 00 is at 15 MHz and points 01 to 10 are spaced at intervals of 100 MHz, starting at 100 MHz and finishing at 1000 MHz. Existing calibration data is shown on the left side of the frequency window in decimal form, new data when it is entered is displayed on the right. Pressing the STORE key transfers the new data to the non-volatile (EAROM) memory.

196. Second function ´193´ Voltage tuned filters (VTF) calibration. The voltage tuned filter (VTF or Output harmonic control) calibration table consists of 6 points running from 500 MHz to 1000 MHz in 100 MHz steps. Display and calibration procedures are identical to those described in the f.m. tracking and r.f. level calibration paragraphs.

197. Second function ´194´ AM calibration. Only two calibration points exist for a.m. Point 00 is calibrated at 15 MHz and point 01 is calibrated at 100 MHz. Calibration is as described in previous paragraphs with the user entering decimal data on the right side of the frequency window then pressing the STORE key to save the new data in the EAROM.

198. Second function ´195´ Calculation and storage of amended EAROM checksum. A check on the serviceability of both PROM and RAM is carried out before the instrument´s initial operating mode is displayed and a checksum is initiated on the EAROM stored data. If either PROM or RAM checks are in error the instrument will be unable to take up the initial operating mode and instead will display an error message, either 06, or 08 depending on the fault. Error messages are described in the Operating Manual Vol. 1. If a new non-volatile EAROM has been fitted or if new r.f. level calibration or f.m. tracking data has been entered (as a result of recalibration) the checksum will not agree and Error number 07 will be displayed in the carrier frequency window until a key is pressed. To recalculate the EAROM checksum enter 2ND FUNC 195 (which will display the current checksum) and press the STORE key. The instrument will re-calculate the checksum, store it in EAROM and display 000 to indicate the completion of the task.

199. Second function ´196´ Protection of store settings. This facility disables the operation of the STORE key in the normal mode of operation in order to provide protection against inadvertent alteration. On selecting second function 196 the frequency window gives a display of either ´0´ to indicate normal operation or ´1´ Stores write-protected. Attempts to overwrite the store contents when protected will result in Error message 18 being displayed in the carrier frequency window.

200. Second function ´197´ Display blanking of recalled stores. This facility enables restrictions to be exercised on the display of data set in stores should this be of a classified nature. Front panel display information is blanked when any store (other than 00) is recalled. All information concerning the existing status, with the exception of error messages and total shift data is prevented from reaching the display. Select ´1´ followed by the STORE key to enable the facility. To disable the facility and return the instrument to the normal display mode press ´0´ and STORE keys. Recall of store 00 will always give a valid display of that stores contents regardless of the state of second function 197 and will also return the instrument to the normal display mode.

201. Second function ´198´ Read total instrument operating time. This read only facility gives the total number of operating hours since instrument manufacture. Selection of this second function will display the record of elapsed time (in hours), in the carrier frequency window with a resolution of 0.5 hrs. When first receiving the instrument a display of time will be evident, reflecting the time spent during manufacture.

Note ...

There is no facility for resetting the total instrument operating time.

202. Second function ´199´ Reset of second function 9 elapsed time. This elapsed time facility can be reset to zero by means of this second function control. When wishing to reset first select second function ´199´ followed by ´0´ and STORE keys.

Chapter 5

MAINTENANCE

CONTENTS

continued ...

CONTENTS (continued)

continued ...

CONTENTS (continued)

INTRODUCTION

1. This chapter contains information for keeping the equipment in good working order, checking overall performance, fault finding and realignment procedures. Before attempting any maintenance on the equipment you are advised to read the preceding chapter containing the technical description.

2. Test procedures described in this chapter may be simplified and of restricted range compared with those that relate to the generally more comprehensive factory test facilities, which are necessary to demonstrate complete compliance with the specifications.

3. Performance limits quoted are for guidance and should not be taken as guaranteed performance specifications unless they are also quoted in the performance data in Chap. 1. When making tests to verify that the instrument meets the stated performance limits, allowance must always be made for the performance of the test equipment used.

4. In case of difficulties which cannot be resolved with the aid of this book, please contact our Service Division at the address given inside the rear cover, or your nearest Marconi Instruments representative. Always quote the type and serial number found on the data plate at the rear of the instrument.

5. Integrated circuit and semiconductor devices are used throughout this instrument and, although these have inherent long term reliability and mechanical ruggedness, they are susceptible to damage by overloading, reverse polarity and excessive heat or radiation and the use of insulation testers.

6. Static sensitive components. ⚠ The c.m.o.s. integrated circuits used in this instrument have extremely high input resistance and can be damaged by accumulation of static charges (see preliminary pages, Notes and Cautions). Boards that have such integrated circuits all carry warning notices against damage by static discharge. Care must also be taken when using freezer sprays to aid fault finding. These can create a static charge likely to change the programmed memory of (E)PROMS.

7. Bulkhead connectors and gaskets. Special care should be taken to ensure that no r.f. leakage occurs. To this end all bulkhead connectors and lid sealing gaskets should be secure. It is essential that the unit lids be

correctly relocated in their slotted recesses after removal. When disconnecting an r.f. connection between units ensure that the metal clad connectors do not accidentally cause short circuits on adjacent p.c.b's. Whenever possible ribbon cable connectors are polarized but care should still be taken to ensure that these are not misplaced. The printed board legends also have a cross hatching printed to indicate the direction by which any given ribbon cable should leave that board.

8. Fault location. This section has been written to assist the user to locate a suspect board and affect a replacement. Recalibration details of these boards are also given in the relevant fault finding table or the Recalibration section. More detailed information is also provided to assist in the isolation of a faulty circuit or component. It is suggested that board replacement be practised as being the most efficient means of maintenance and repair, see para. 47 for details.

PERFORMANCE CHECKS

Overall tests and adjustments

9. Many of the tests described in this chapter are simplified and of restricted range compared with those which would demonstrate compliance with the specification as described in paras. 1 to 4. If the results quoted in the following paragraphs are not obtainable refer to the related fault finding section and tables, and after repair ensure that re-alignment is carried out in accordance with that section, if applicable.

Note ...

Voltages quoted alongside power levels are e.m.f. values. Thus the voltage developed across a 50 Ω load will be one half of the values given.

TABLE 1 TEST EQUIPMENT

Item	Description	Measurement requirements	Recommended model
a	Modulation meter with distortion measuring facility	Range ΦM:0.01 to 9.99 radians FM: 10 Hz to 99.9 kHz AM: 0 to 99.5% Accuracy FM & ΦM: ±5% of deviation at 1 kHz AM: ±4% of depth setting +1% Distortion AM,FM & ΦM: <5% total harmonic distortion	2305 & Distortion options kit (or TF 2331A)
b	Frequency counter	Freq. range: 10 kHz to 1 GHz Accuracy: Better than ±2 in 10^7 over the temperature range 0 to 40^0C	2435

continued ...

TABLE 1 TEST EQUIPMENT (continued)

Item	Description	Measurement requirements	Recommended model
c	Standard frequency source (1,5 or 10 MHz)	Output level: >1 V r.m.s.	Rubidium or Caesium reference unit
d	RF Power Meter with Power Sensor	Output level: -127 dBm to +6 dBm Level accuracy: ±1 dB from 10 kHz to 1 GHz	6960 & 6912
e	AC Voltmeter	Output level: 1 V ±10% e.m.f.	2610
f	AF Signal Source	Frequency range: 50 Hz - 25 kHz Output level: 0.90-1.10 V	Any suitable model
g	RF Millivoltmeter	VSWR: <1.5:1 Freq. range: 10 kHz-350 MHz	TF 2603
h	T Connector	VSWR: <1.5:1 Freq. range: 10 kHz-350 MHz	TM 7984
i	N type 50 Ω load	VSWR: <1.5:1 Freq. range: 10 kHz-350 MHz	TM 7967
j	Short circuit monitor	VSWR: <1.5:1 Freq. range: 350-1000 MHz	See Fig. 9a
k	20 c.m. Air spaced line	VSWR: <1.5:1 Freq. range: 350-1000 MHz	GR 874-L20
l	20 c.m. Adjustable line	VSWR: <1.5:1 Freq. range: 350-1000 MHz	GR 874-LK20L
m	DC microvoltmeter	Voltage range : ±3 µV f.s.d.	LEVELL Type TM8
n	Spectrum analyzer	Freq. range: 15 MHz-1.5 GHz	
o	Variable d.c. power supply	Voltage: ±5 V	TF 2158
p	Distortion factor meter	Distortion AM,FM & ΦM: <5% total harmonic distortion Distortion MOD OSC: <1% total harmonic distortion	TF 2331A

TABLE 2 DECIBEL CONVERSION TABLE

Ratio down			Ratio up	
Voltage	Power	Decibels	Voltage	Power
1.0	1.0	0	1.0	1.0
.9886	.9772	.1	1.012	1.023
.9772	.9550	.2	1.023	1.047
.9661	.9333	.3	1.035	1.072
.9550	.9120	.4	1.047	1.096
.9441	.8913	.5	1.059	1.122
.9333	.8710	.6	1.072	1.148
.9226	.8511	.7	1.084	1.175
.9120	.8318	.8	1.096	1.202
.9016	.8128	.9	1.109	1.230
.8913	.7943	1.0	1.122	1.259
.8710	.7586	1.2	1.148	1.318
.8511	.7244	1.4	1.175	1.380
.8318	.6918	1.6	1.202	1.445
.8128	.6607	1.8	1.230	1.514
.7943	.6310	2.0	1.259	1.585
.7762	.6026	2.2	1.288	1.660
.7586	.5754	2.4	1.318	1.738
.7413	.5495	2.6	1.349	1.820
.7244	.5248	2.8	1.380	1.905
.7079	.5012	3.0	1.413	1.995
.6683	.4467	3.5	1.496	2.239
.6310	.3981	4.0	1.585	2.512
.5957	.3548	4.5	1.679	2.818
.5623	.3162	5.0	1.778	3.162
.5309	.2818	5.5	1.884	3.548
.5012	.2512	6	1.995	3.981
.4467	.1995	7	2.239	5.012
.3981	.1585	8	2.512	6.310
.3548	.1259	9	2.818	7.943
.3162	.1000	10	3.162	10.000
.2818	.07943	11	3.548	12.59
.2512	.06310	12	3.981	15.85
.2239	.05012	13	4.467	19.95
.1995	.03981	14	5.012	25.12
.1778	.03162	15	5.623	31.62

TABLE 2 DECIBEL CONVERSION TABLE (continued)

Ratio down			Ratio up	
Voltage	Power	Decibels	Voltage	Power
.1585	.02512	16	6.310	39.81
.1413	.01995	17	7.079	50.12
.1259	.01585	18	7.943	63.10
.1122	.01259	19	8.913	79.43
.1000	.01000	20	10.000	100.00
.07943	6.310×10^{-3}	22	12.59	158.5
.06310	3.981×10^{-3}	24	15.85	251.2
.05012	2.512×10^{-3}	26	19.95	398.1
.03981	1.585×10^{-3}	28	25.12	631.0
.03162	1.000×10^{-3}	30	31.62	1,000
.02512	6.310×10^{-4}	32	39.81	1.585×10^{3}
.01995	3.981×10^{-4}	34	50.12	2.512×10^{3}
.01585	2.512×10^{-4}	36	63.10	3.981×10^{3}
.01259	1.585×10^{-4}	38	79.43	6.310×10^{3}
.01000	1.000×10^{-4}	40	100.00	1.000×10^{4}
7.943×10^{-3}	6.310×10^{-5}	42	125.9	1.585×10^{4}
6.310×10^{-3}	3.981×10^{-5}	44	158.5	2.512×10^{4}
5.012×10^{-3}	2.512×10^{-5}	46	199.5	3.981×10^{4}
3.981×10^{-3}	1.585×10^{-5}	48	251.2	6.310×10^{4}
3.162×10^{-3}	1.000×10^{-5}	50	316.2	1.000×10^{5}
2.512×10^{-3}	6.310×10^{-6}	52	398.1	1.585×10^{5}
1.995×10^{-3}	3.981×10^{-6}	54	501.2	2.512×10^{5}
1.585×10^{-3}	2.512×10^{-6}	56	631.0	3.981×10^{5}
1.259×10^{-3}	1.585×10^{-6}	58	794.3	6.310×10^{5}
1.000×10^{-3}	1.000×10^{-6}	60	1,000	1.000×10^{4}
5.623×10^{-4}	3.162×10^{-7}	65	1.778×10^{3}	3.162×10^{4}
3.162×10^{-4}	1.000×10^{-7}	70	3.162×10^{3}	1.000×10^{7}
1.778×10^{-4}	3.162×10^{-8}	75	5.623×10^{3}	3.162×10^{7}
1.000×10^{-4}	1.000×10^{-8}	80	1.000×10^{4}	1.000×10^{8}
5.623×10^{-5}	3.162×10^{-9}	85	1.778×10^{4}	3.162×10^{8}
3.162×10^{-5}	1.000×10^{-9}	90	3.162×10^{4}	1.000×10^{9}
1.000×10^{-5}	1.000×10^{-10}	100	1.000×10^{5}	1.000×10^{10}
3.162×10^{-6}	1.000×10^{-11}	110	3.162×10^{5}	1.000×10^{11}
1.000×10^{-6}	1.000×10^{-12}	120	1.000×10^{6}	1.000×10^{12}
3.162×10^{-7}	1.000×10^{-13}	130	3.162×10^{6}	1.000×10^{13}
1.000×10^{-7}	1.000×10^{-14}	140	1.000×10^{7}	1.000×10^{14}

Frequency accuracy

10.

TEST EQUIPMENT
(a) Frequency Counter 2435

2022 PERFORMANCE DATA
Freq. range: 10 kHz to 1 GHz.
Accuracy: Equal to freq. std.

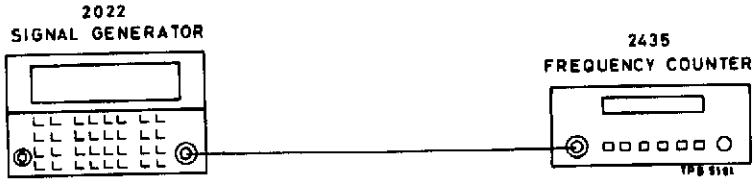


Fig. 1 Test gear arrangement to check frequency accuracy

Procedure

(1) Connect test equipment as shown in Fig. 1 and set the 2022 control as follows:-

CARR FREQ : 10 kHz
AM : OFF
FM/ϕM : OFF
RF LEVEL : -10 dB

(2) Carry out spot checks throughout the range of the instrument ensuring that frequencies can be selected correctly and that they are within specification.

(3) If wishing to check using an external frequency standard, connect this to the rear panel mounted STD FREQ IN socket. One of three frequencies can be used 1,5 or 10 MHz, provided that an internal link selection within the 2022 corresponds to the frequency of the external standard. An indication of the link setting is given when Second function 1 'Status' mode is selected. Here either a 1,5 or 10 notation is displayed in the modulation window. Instructions on changing the link setting are given in the Re-calibration section of this chapter.

(4) The level of an external frequency standard should be greater than 1 V r.m.s.

RF output

11.

TEST EQUIPMENT
(d) RF Power Meter 6960 and Power Sensor 6912

2022 PERFORMANCE DATA	
Level:	-127 dBm to +6 dBm
Level accuracy:	1 dB from 10 kHz - 1 GHz (above -10 dBm).
:	±2 dB from 10 kHz - 1 GHz (below -10 dBm).

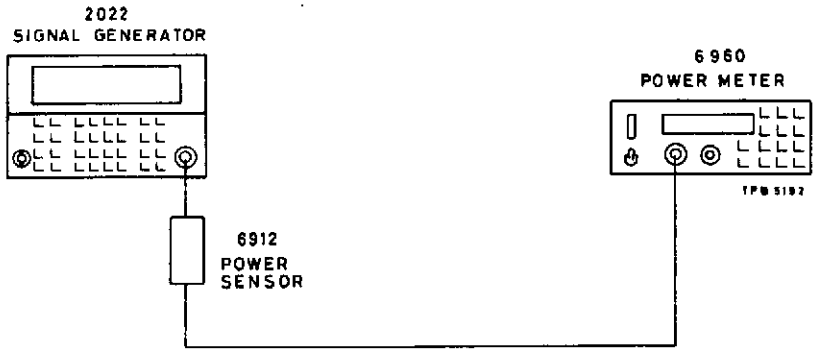


Fig. 2 Test gear arrangement to check RF output

Procedure

(1) Connect test equipment as shown in Fig. 2 and set the 2022 controls as follows:-

CARR FREQ : 500 MHz
AM : OFF
FM/ΦM : OFF
RF LEVEL : -10 dBm (141 mV)

(2) Note the power reading at -10 dBm and check that this is within specification. Maintain this level setting and select other carrier frequencies e.g. 100 kHz, 1 MHz, 100 MHz and 1000 MHz.

(3) Further check other level settings up to a maximum of +6 dBm (892 mV).

12. The 10 dB step attenuator AC0 contains three 30 db pads, one 20 dB pad and one 10 dB pad. Each of these may be selected individually by utilizing the Second function 3 mode. Levels below -10 dBm can best be checked by this method as follows:-

(1) Set the 2022 RF OUTPUT to +6 dBm and set a reference level of 0 dB on the Power Meter 6960. AC0, step attenuator is controlled from A2 board address 05. To select each relay in turn enter by means of the keyboard controls Second function 3, then 05. If unfamiliar with this procedure see 'Use of second function 3' (Manual latch setting) paragraphs included later in this chapter.

(2) The data showing in the Frequency window is that which is currently addressed to the attenuator latch in binary notation. Enter new data by means of '1' or '0' numerals via the instrument keyboard. Numbers are rotated in from the right. When the data is set press the STORE key and the appropriate relay will energize. See Table 3 below for each attenuator relay selection.

TABLE 3 AC0/AC1 ATTENUATOR CHECK

Binary number						Relay	Attenuation
D5	D4	D3	D2	D1	D0	energized	
0	1	1	1	1	0	RLA	30 dB
0	1	1	1	0	1	RLB	20 dB
0	1	1	0	1	1	RLC	30 dB
0	1	0	1	1	1	RLD	10 dB
0	0	1	1	1	1	RLE	30 dB

(3) Check that the output falls to the appropriate level on the power meter as each attenuator pad is selected. Typical accuracy expected is as follows, 10 dB, 0.2 dB; 20 dB, 0.25 dB and 30 dB, 0.3 dB.

(4) A spectrum analyzer may be used as an alternative to check levels down to -90 dBm with limited accuracy.

Modulation oscillator performance

13.

TEST EQUIPMENT
(b) Frequency Counter 2435
(e) True RMS Voltmeter 2610
(p) Distortion Factor Meter TF 2331A

2022 PERFORMANCE DATA	
Freq.:	1 kHz
Accuracy:	Equal to freq. std. accuracy
Distortion:	<1% total harmonic distortion
Output level:	1 V 10% e.m.f. from a nominal 600 Ω source impedance.

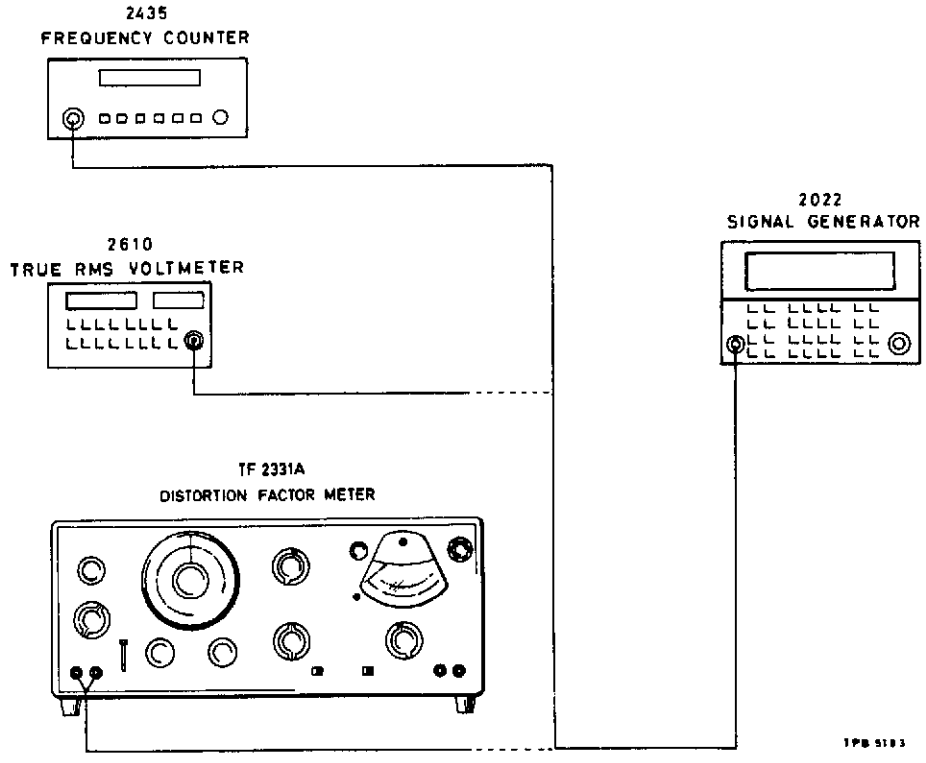


Fig. 3 Test gear arrangement to check Mod. osc. performance

Procedure

(1) Connect test equipment as shown in Fig. 3 and set the 2022 controls as follows:-

FM/ϕM : FM
MOD ON/OFF : ON

(2) Check that the frequency of the MOD IN/OUT signal is within specification.

(3) Remove the frequency counter and connect the voltmeter to the 2022 MOD IN/OUT socket and check that the output level is within specification.

(4) Remove the voltmeter and connect the distortion factor meter and check that distortion is within specification.

FM deviation and distortion

14.

TEST EQUIPMENT
(a) Modulation Meter 2305 with Distortion options kit

2022 PERFORMANCE DATA	
Range:	10Hz to 99.9kHz peak deviation.
Deviation accuracy:	±5% of deviation at 1kHz mod. freq. excluding residual f.m.
Distortion:	<5% total harmonic distortion at 1 kHz mod. freq. and max. deviation for any carr. freq. above 250 kHz.

Fig. 4 Test gear arrangement to check f.m. deviation and distortion

Procedure

(1) Connect test equipment as shown in Fig. 4 and set the 2022 controls as follows:-

CARR FREQ : 250 MHz
FM/ΦM : FM
Deviation : 99.9 kHz
RF LEVEL : 0 dBm

(2) Select 2305, 50 Hz - 15 kHz filter and check that the indicated deviation is within specification allowing for the effects of residual f.m.

(3) Select 2305, DIST function key and check that the indicated distortion reading is within specification.

(4) Repeat steps (2) and (3) with further deviation settings of 100 Hz, 1 kHz and 10 kHz.

(5) Repeat steps (2), (3) and (4) with additional carrier frequency selections of 350, 360 and 499 MHz.

Phase modulation and distortion

15.

TEST EQUIPMENT
(a) Modulation Meter 2305 with Distortion options kit.

2022 PERFORMANCE DATA	
Range:	0.01 to 9.99 radians.
Deviation accuracy:	±5% of deviation at 1 kHz mod. freq. excluding residual phase mod.
Distortion:	<5% total harmonic distortion at 1 kHz mod. freq and max. dev. at any carrier freq. above 250 kHz.

Fig. 5 Test gear arrangement to check phase mod. and distortion

Procedure

(1) Connect test equipment as shown in Fig. 5 and set the 2022 controls as follows:-

CARR FREQ: 250 MHz
FM/ΦM: ΦM
Deviation: 9.99 Radians
RF LEVEL: 0 dBm

Because ΦM and FM mostly share common circuitry it is necessary to check only one deviation setting.

(2) Select 2305 ΦM function key and check that the deviation reading is within specification.

(3) Select 2305 DIST function key and measure the distortion, check that this is within specification.

AM depth and distortion (Internal)

16.

TEST EQUIPMENT
(a) Modulation Meter 2305 with Distortion options kit.

2022 PERFORMANCE DATA	
Range:	0 to 99.5%.
Accuracy:	±4% of depth setting +1% for 1 kHz mod. freq. and depths up to 95% for carrier freqs. up to 62.5 MHz (80% for carrier freqs. up to 400 MHz).
Freq. response:	±1 dB from 50 Hz - 15 kHz.
Distortion:	<5% total harmonic distortion for depths 0-95% for carrier freqs. up to 62.5 MHz and 0-80% for carrier freqs. up to 400 MHz.

Fig. 6 Test gear arrangement to check a.m. depth and distortion

Procedure

(1) Connect test equipment as shown in Fig. 6 and set the 2022 controls as follows:-

CARR FREQ:	15 MHz
AM:	ON
Modulation:	95%
RF LEVEL:	0 dBm

A fixed frequency modulator is used to provide the modulation at carrier frequencies below 62.5 MHz and envelope feedback is used for carrier frequencies above 62.5 MHz.

(2) Select 2305, 50 Hz to 15 kHz filter and AM function key. Check that the displayed reading is within specification.

(3) Select 2305, DIST function key and measure the distortion and check that this is within specification.

(4) Reset 2022 controls:-

CARR FREQ:	200 MHz
AM:	ON
Modulation:	80%
RF LEVEL:	0 DBM

17. Again check the depth and distortion as described in steps (2) and (3) using the 2305.
Finally repeat step (4) with the RF LEVEL setting reduced to -10 dBm, readings should remain unchanged.

External modulation (ALC ON)

18.

TEST EQUIPMENT
(a) Modulation Meter 2305
(e) True RMS Voltmeter 2610
(f) AF Signal Source (low distortion)

2022 PERFORMANCE DATA	
Input level:	Dev. is calibrated for input levels between 0.9 V and 1.1 V r.m.s. HI or LO l.e.d's indicate if outside this range.
Freq. response: (relative to 1 kHz mod. with ALC ON).	AM 1 dB from 50 Hz to 15 kHz FM 1 dB from 50 Hz to 25 kHz ΦM ±1 dB from 50 Hz to 10 kHz

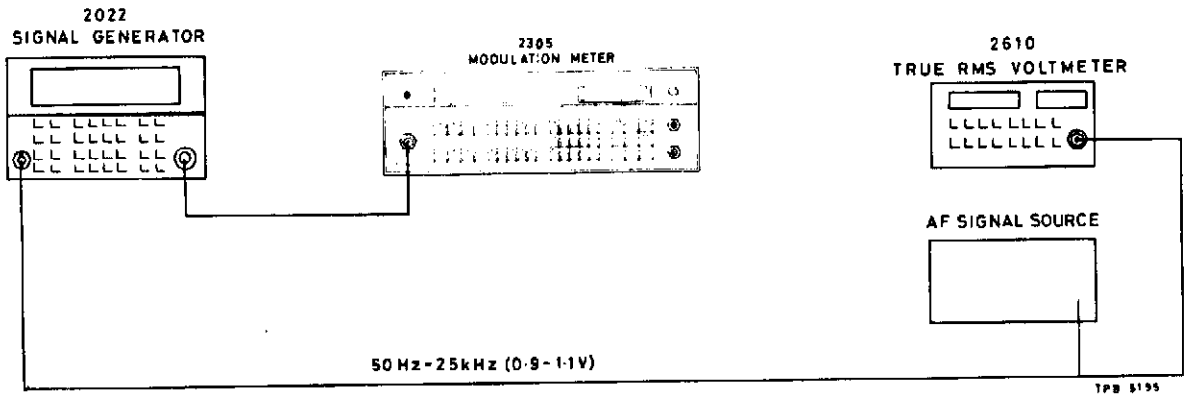


Fig. 7 Test gear arrangement to check external modulation

Procedure

(1) Because AM, FM and ΦM external modulation use a common circuit configuration, checking need only be carried out with one type of modulation input. Connect the test equipment as shown in Fig. 7 and set the 2022 controls as follows:-

CARR FREQ: 250 MHz
FM/ΦM: FM
INT/EXT: EXT
Deviation: 99.9 kHz
MOD ALC: ON (l.e.d. lit)

(2) Apply a 1 kHz, 1.00 V r.m.s. input from a low distortion AF signal source to the 2022 MOD IN-OUT socket.

(3) Select 2305, 30 - 50 kHz filter and FM function key. Check that the displayed f.m. deviation reading is within specification.

(4) Vary the input voltage between 0.9 V and 1.1 V and check that the modulation display does not indicate either a HI or LO message. Also check that the deviation remains constant over the range.

(5) Select 2305 REL function key and vary the frequency of the external mod. signal between 50 Hz and 25 kHz. Check that the deviation remains within ±1 dB of the value set at 1 kHz mod. frequency.

(6) Select 30% a.m. and repeat step (5) for external modulation signals varying from 50 Hz to 15 kHz. Check that the modulation depth remains within 1 dB of the value set at 1 kHz modulating frequency.

External modulation (ALC off)

19. (1) Connect test equipment as shown in the previous figure. Maintain 2022 settings with the exception of the MOD ALC key. Press this to disable the ALC (adjacent l.e.d. should be extinguished).

(2) Select 2305, ABS function key and apply a 1 kHz, 1.00 V r.m.s. signal to the MOD IN-OUT socket of the 2022. Check that the f.m. deviation displayed on the 2305 is within specification.

VSWR (50 kHz - 350 MHz)

20.

TEST EQUIPMENT
(g) RF Millivoltmeter TF 2603
(h) T connector, TM 7984
(i) N type 50 Ω load TM 7967

2022 PERFORMANCE DATA
VSWR: <1.5:1 for output levels below -10 dBm

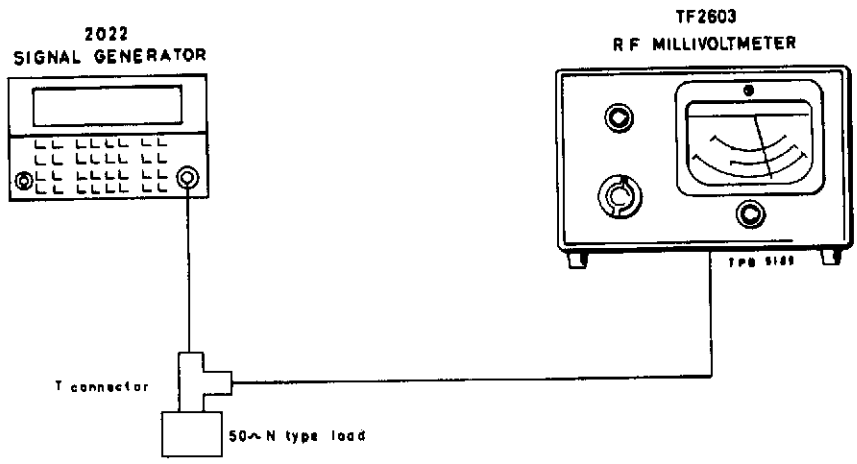


Fig. 8 Test gear arrangement to check v.s.w.r. up to 350 MHz

Procedure

(1) Connect test equipment as shown in Fig. 8 and set the 2022 controls as follows:-

CARR FREQ: 100 MHz
RF LEVEL: -10 dBm (141 mV)

(2) With the 50 Ω load disconnected note the reading in the TF 2603.

(3) Now insert the 50 Ω load, note the new reading. The impedance, Z is calculated using the following formula,

$$Z = \frac{50\ E}{V} - 50\ \Omega$$

Where E = open circuit output level
and V = output across the 50 Ω load

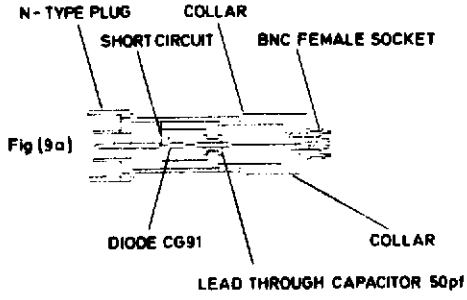
From the above, v.s.w.r. = $\frac{Z}{50}$ or $\frac{50}{Z}$ and should be better than 1.5:1.

VSWR (above 350 MHz)

21.

TEST EQUIPMENT
(j) Short circuit monitor
(k) 20 cm Air spaced line GR 874-L20
(l) 20 cm Adjustable line GR 874-LK20L
(m) DC microvoltmeter

2022 PERFORMANCE DATA
VSWR: 1.5:1 for output levels below -10 dBm



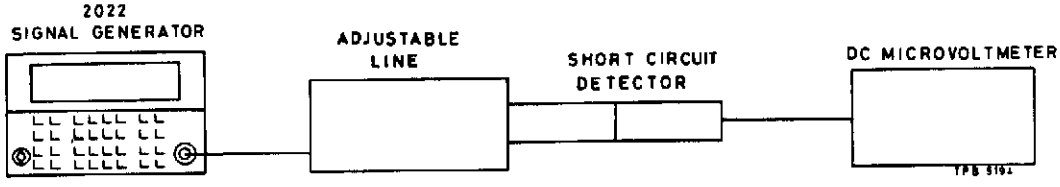


Fig. 9 Test gear arrangement to check v.s.w.r. above 350 MHz

(1) Connect the test equipment as shown in Fig. 9 and set the 2022 controls as follows:-

CARR FREQ: 500 MHz
RF LEVEL: -10 dBm (141 mV)

(2) Set the adjustable line to 1/2 λ of the signal by applying the formula $\lambda = \frac{300}{f}$

Where λ is the wavelength in metres
and f is the frequency in MHz,

e.g. at 500 MHz, $\lambda = \frac{300}{500} = 0.6$ m

1/2 λ = 30 cm.

(3) Adjust the line length for maximum indication on the meter and note the reading. Adjust the line length for minimum indication in the meter (1/4 λ).

Note ...

The short circuit current monitor uses a diode to detect the maximum and minimum values (Vmax. and Vmin.) This diode is being used at the lowest part of its characteristic and the square law applies.

The v.s.w.r. is therefore equal to $\sqrt{\frac{Vmax.}{Vmin.}}$ and should be better than 1.5:1.

Carrier harmonics and sub-harmonics

22.

TEST EQUIPMENT
(n) Spectrum analyzer

2022 PERFORMANCE DATA	
1. Harmonically related signals for output levels below 0 dBm:	Better than -25 dBc for any carrier freq.
2. Sub-harmonics for output levels below 0 dBm:	None for carrier freqs. below 500 MHz. -20 dBc above 500 MHz.
3. Non-harmonically related signals for output levels below 0 dBm:	<-70 dBc for carrier freqs. of 62.5 MHz and above. <-55 dBc below 62.5 MHz in the band up to 150 MHz and <-40 dBc above 150 MHz.

Fig. 10 Test gear arrangement to check carrier harmonics and sub-harmonics

Procedure

(1) Connect the test equipment as shown in Fig. 10 and set the 2022 controls as follows:-

RF LEVEL: 0 dB
CARR FREQ: 15 MHz
AM,FM,ΦM: OFF

(2) The spectrum analyzer used should be capable of measuring at least the 3rd harmonic of the carrier frequency. Check that the amplitude of any harmonic does not exceed specification at carrier frequencies of 15,63,126,252,300 and 500 MHz. Repeat these checks with further r.f. level settings of +6 dBm and -10 dBm. The carrier frequencies selected will check for harmonics in the following circuits,

15 MHz	BFO band
63 MHz	Incorporates two stages of freq. division
126 MHz	Uses a single divider stage
252 MHz	Fundamental band
300 MHz 350 MHz	} Checks the tracking of the tuning notch
500 MHz	Doubler band

(3) Sub-harmonics are only produced when carrier frequencies above 500 MHz are selected. Check at the three r.f. level settings given; 0 dBm, +6 dBm and -10 dBm, that the sub-harmonics do not exceed specifications at each of the following carrier frequencies 501 MHz, 700 MHz, 900 MHz and 1000 MHz.

Residual f.m.

23.

TEST EQUIPMENT
(a) Modulation Meter 2305
(e) True RMS Voltmeter 2610

2022 PERFORMANCE DATA	
Residual f.m.	<20 Hz equiv. peak dev. in a 300 Hz - 3 kHz bandwidth at 499 MHz and improving by approx. 6 dB/octave with reducing carrier freqs. down to 62.5 MHz. <10 Hz below 62.5 MHz.

Fig. 11 Test gear arrangement to check residual f.m.

Procedure

(1) Connect the test equipment as shown in Fig. 11 and select the 2305, 300 Hz - 3.4 kHz filter, noise averaging and function switch to f.m.

(2) Set the 2022 controls as follows :-

CARR FREQ : 250 MHz
RF LEVEL : 0 dBm
MOD ON/OFF : OFF

(3) Using the 2305, measure the residual f.m. at frequencies given in Table 4 and ensure that the instrument is within specifications.

TABLE 4 RESIDUAL FM DEVIATION DATA

Carrier freq.	Specification
50 MHz	10.0 Hz
250 MHz	7.5 Hz
352 MHz	10.0 Hz
354 MHz	10.0 Hz
499 MHz	15.0 Hz

Reverse power protection

24.

TEST EQUIPMENT
(e) True RMS Voltmeter 2610
(o) Variable d.c. power supply TF 2158

2022 PERFORMANCE DATA	
Protection:	The generator output is protected against reverse power of up to 25 W from d.c. to 1 GHz.

Procedure

(1) Switch 2022 power-on to internally connect the output socket of the instrument. Set the RF LEVEL to 0 dBm (This will protect the resistors in the attenuator in the event of an RPP malfunction). Then set the d.c. power supply to +5 V and apply this to the 2022 RF OUTPUT 50 Ω socket causing the RPP circuit to trip (taking care not to damage the connector pin).

(2) An indication that the reverse power unit has been tripped will now be given by the REV PWR annunciator which will flash on the RF LEVEL display.

(3) Remove the +5 V source and check that there is no continuity between the 'N' type connector centre pin and earth (again taking care not to damage the connector pin). If the RPP has not tripped, a resistance of approximately 1 kΩ may be measured between the centre pin and earth.

(4) Reset the RPP by pressing the RF LEVEL key and ensure that the REV PWR indication is now off. Set the d.c. power supply to -5 V and apply this again to the RF OUTPUT 50 Ω socket checking that the RPP trips once more. Remove the d.c. source and reset the RPP.

(5) Operation of the RPP trip circuit can also be checked if required without the application of a voltage to the RF OUTPUT 50 Ω socket using Second function 3 (Manual latch setting). Access to the attenuator latch for AC0 and the means of entering the necessary data to achieve this is described in para. 12. Setting a binary '1' level in D5 (see Table 3) will cause the RPP to trip.

FAULT LOCATION

Introduction

25. This section consists of fault finding procedures and tests to aid fault analysis. It is advisable to study the description of the overall instrument contained in Chap. 4. The functions of each board are generally well defined and independent of each other as far as possible. All boards are interconnected by a variety of connectors. The recommended method of confirming a board fault is to substitute the unit with a unit that is known to be good (e.g. from a spare serviceable instrument). This can save considerable fault finding time.

26. Easily accessible test points are provided on the boards to allow the user to quickly confirm that voltage rails are correct. These are simply solder pads with a central hole surrounded by a white circle. The nominal voltage expected at that point is also indicated as shown in Fig. 12 below

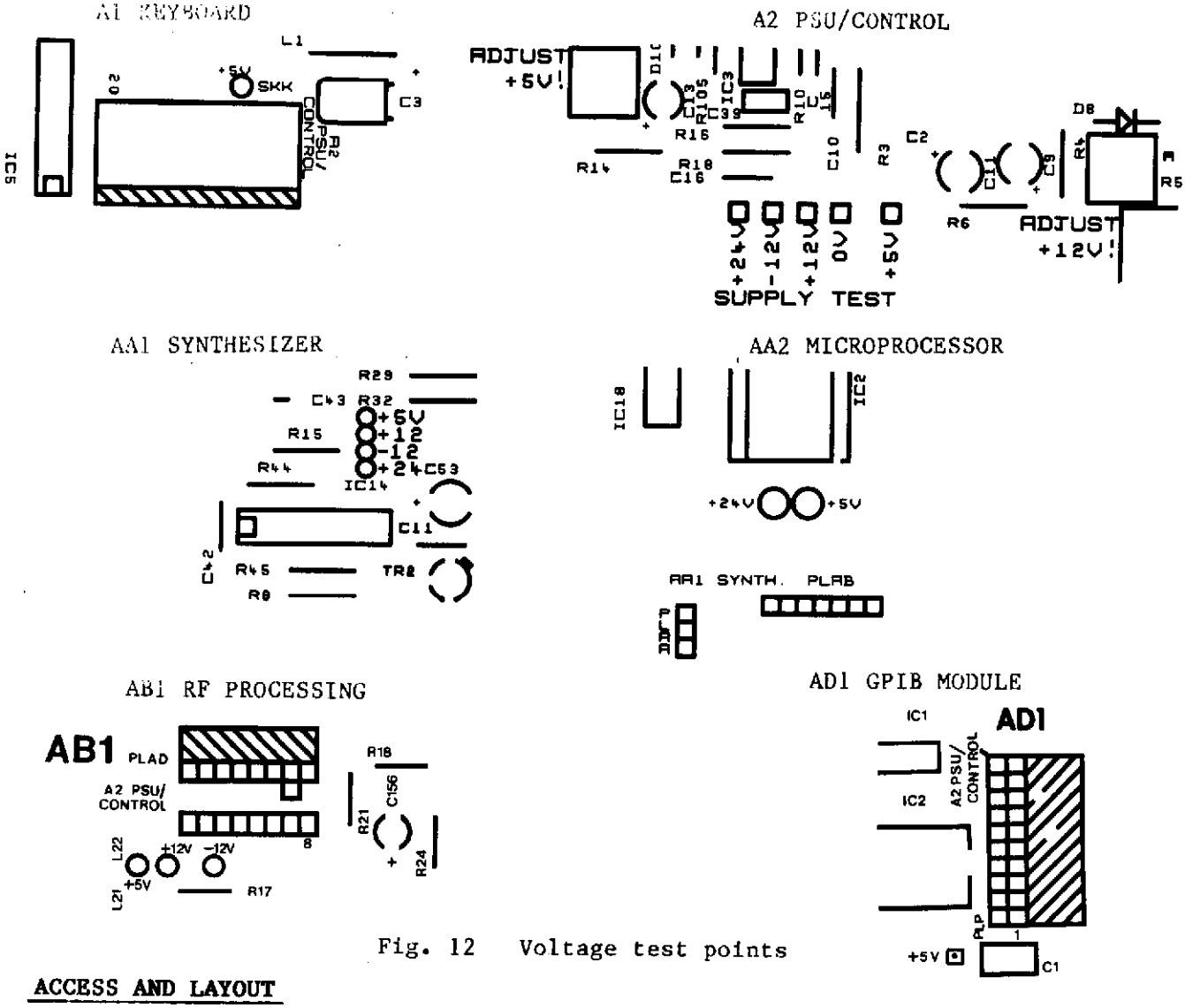


Fig. 12 Voltage test points

ACCESS AND LAYOUT

27. Access to the interior of the instrument can be gained by first removing the rear casting which is retained by two centre fixing cross headed screws. Both top and bottom outer covers can then be removed.

Access to AA1 and AA2 boards

28. Remove eight of the screws that secure AA0 cover plate. There are five screws on either side of the unit but the two centrally mounted ones should not be removed because they secure AA0 unit to the side-frames (see Fig. 13a for details). AA0 cover plate can now be raised to access board AA2 which is attached to the underside of AA0 cover plate. Board AA1 is situated inside AA0 unit.

29. If it is required to remove AA2 then connectors PLAA, PLAB and PLAC should be detached from the board otherwise the cover plate can be rotated through 180° and secured with two screws into the servicing position as shown in Fig. 13a.

Access to AB1 board and removal of AB0 unit

30. Place the instrument upside down and remove the eight outermost fixing screws (shown in Fig. 13a). Remove the cover plate which will give access to board AB1.

31. The two remaining centrally mounted fixing screws secure AB0 unit to the side frames. To remove AB0, unscrew the two remaining centrally mounted fixing screws and conhex connectors SKW and SKZ. Raise AB0 unit at the rear of the instrument, pivoting about the front edge until it is possible to remove sockets SKN and SKM from A2 board. Finally remove the RF output connector, PLAF from the attenuator and withdraw AB0 unit. When replacing AB0 unit, ensure that the GPIB module AD0 is correctly located between the two guides on the underside of AB0. If difficulty is experienced, remove AD0 (see para. 33) before attempting to replace AB0.

Access and removal of A2, Power supply and Control board

32. Access to this board is achieved by removing AB0 unit as described in the previous paragraph. To remove A2 p.c.b., disconnect the sockets from the following plugs, PLF, PLH, PLAG, PLJ, PLL and PLK, then disconnect SKP from the GPIB module AD0. The board can then be released from the instrument after removing the nine fixing screws.

33. Before access can be gained to the components on the rear panel AD0, GPIB module, (if fitted), must be withdrawn from the instrument. Remove the two cross headed screws securing the module to the rear panel. Carefully slide out the board assembly from the instrument as shown in Fig. 13b. Also withdraw the interconnecting lead and disconnect SKP socket from the GPIB module.

34. Remove the two upper screws that secure the rear panel to the side frame and loosen only the two lower securing screws as shown in Fig. 13d. The rear panel can now be partially hinged to allow access to SKR, STD FREQ IN socket, detach this and the rear panel is then free to angle down.

Note ...

When replacing AD0, GPIB module attach the interconnecting lead and socket SKP to the rear of the board. Then slide the unit into the instrument ensuring that the component side of board AD1 is facing the side frame of the instrument. Also check that the board locates correctly between the guides shown in Fig. 13b.

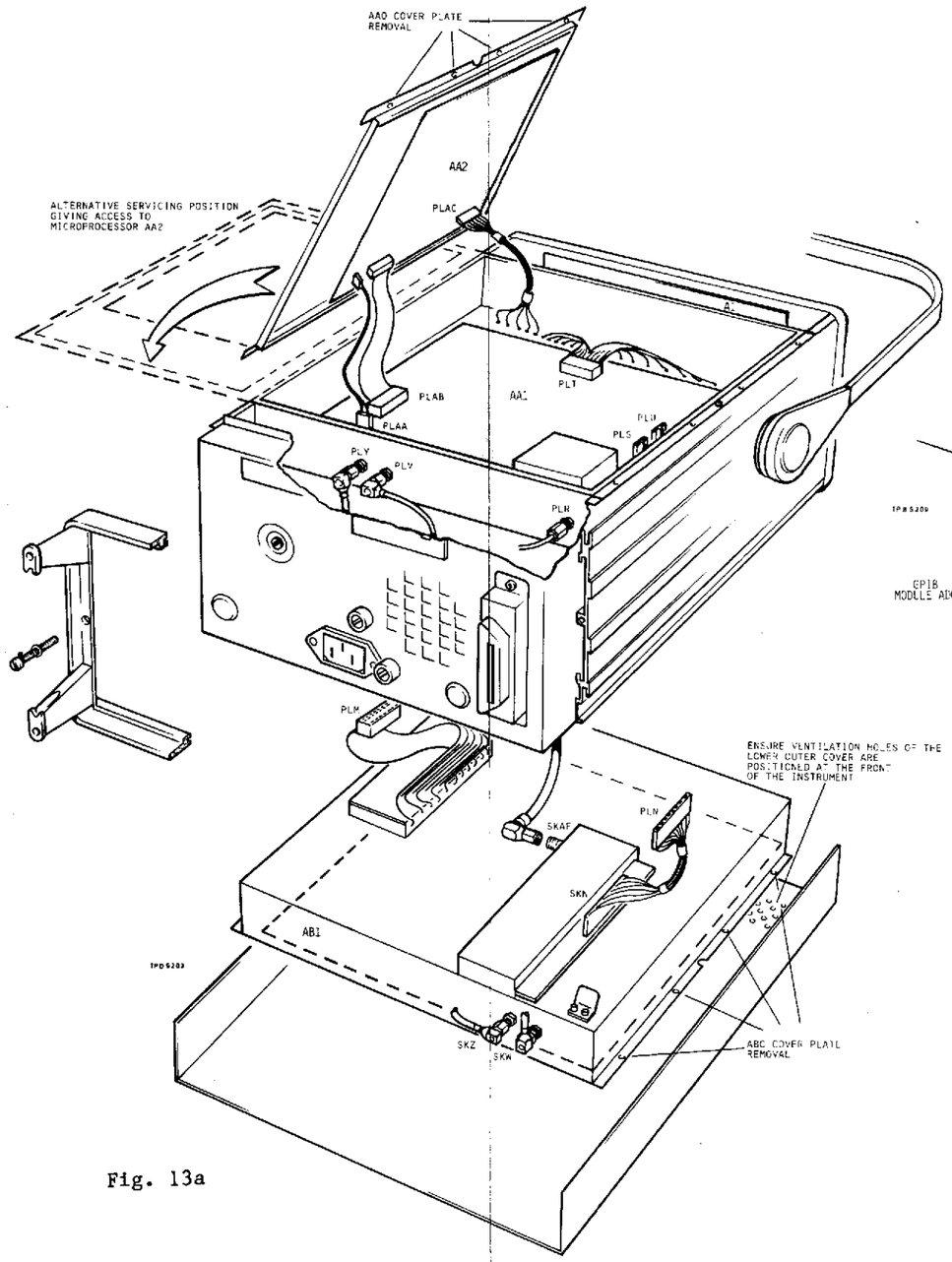


Fig. 13a

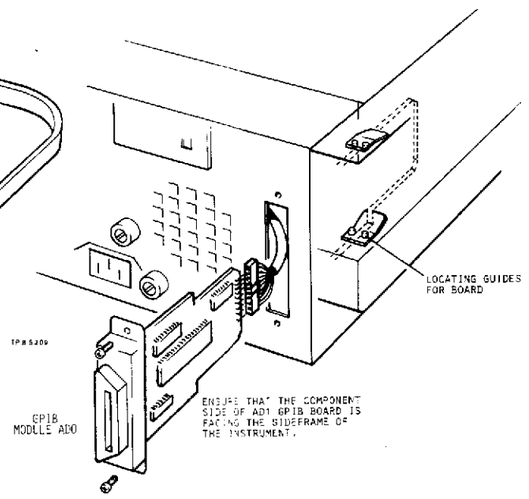


Fig. 13b

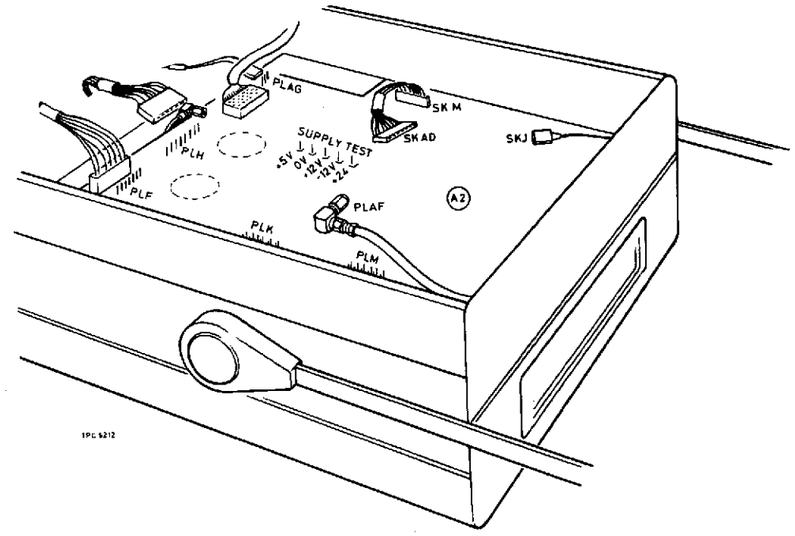


Fig. 13c

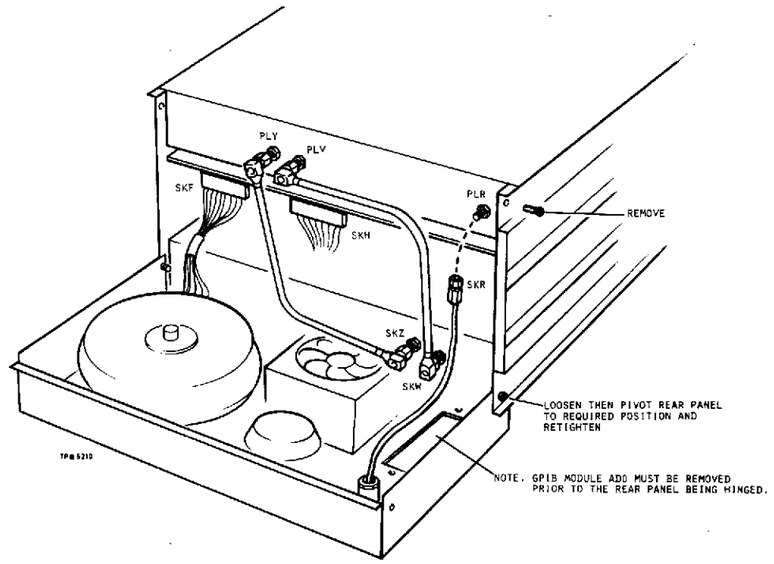


Fig. 13d

Fig. 13 Access and layout

Access and removal of A1 keyboard

35. Limited access to the keyboard can be obtained without removing either AA0 or AB0 units. First ensure that the a.c. supply is disconnected from the instrument. Now remove the two outer instrument covers and then the four screws (two in each side frame) securing the front panel to the side frame. Turn the instrument upside down and remove the nut securing the SUPPLY ON-OFF switch. Push the switch back through the front panel. Disconnect the MOD IN-OUT socket SKJ from A2 board. It is now possible to hinge the front panel about the side of the RF OUTPUT socket. Access can now be gained to the rear of A1 keyboard which can be removed after withdrawing six cross headed securing screws.

Rear panel mounting for RF OUTPUT and MOD IN-OUT sockets

36. General instructions for rack mounting are given in Chap. 2, Vol. 1 of the Operating Manual. If in addition it is required to mount the RF OUTPUT and MOD IN-OUT sockets to the rear panel this can be facilitated easily without recourse to additional wiring. Two front panel blanking grommets are supplied to insert in the vacated positions if required.

37. First remove AB0 RF unit as described in previous paragraphs. Now remove the four cross headed screws securing the front panel to the side frames and disconnect socket SKK from A2 board. The front panel can now be hinged to allow access and subsequent removal of SKJ, MOD IN-OUT connector from A2 board. Keyboard A1 can now be removed from the front panel support by removing the six cross headed screws. Access to the RF OUTPUT and MOD IN-OUT sockets is now possible. Unfasten the two retaining nuts holding the sockets to the front panel and the earth tag from alongside the MOD IN-OUT socket.

38. Additional coaxial cable is coiled and cleated between A1 keyboard and the front panel support. Uncleat this and re-route the connector alongside the side frame with the mains supply lead. Remove and discard the rear panel blind grommet and secure the MOD IN-OUT socket to the rear panel using the existing nut. A suitable stud is provided next to the sockets position for fixing the earth braid tag.

39. The RF OUTPUT socket is simply re-connected to the rear panel position after removing and discarding the blind grommet. The front panel unit can now be re-assembled and AB0 unit can be refitted and connected up.

USE OF 2ND FUNCTION 3 (MANUAL LATCH SETTING)

Data entry (6 and 8-bit)

40. This unprotected second function control allows the user to enter data to any specified latch directly (with the exception of the l.c.d's on keyboard A1 which has an alternative second function control of its own). The data will remain valid until the manual latch addressing mode is terminated by pressing one of the main function keys. Then all normal latch data will be reinstated. See also Chap. 4 Second function operations for further details of 2ND FUNCT 3. Each latch is identified on the circuit diagram with an address number e.g. 03, 05 etc. See Table 5 for details of all available address numbers and latch descriptions. Two formats must be considered; 6-bit data and 8-bit data.

41. 6-bit data. Having determined from the circuit diagram that the latch of interest to be addressed has 6 bits, data in the form of ones or zero's

should be entered until six segments of the frequency display are occupied. To do this select 2ND FUNCT '3' then, using the keyboard controls, select the required address. Data presented on the frequency display will be that which is addressed to the latch at the present time.

42. The required data can now be entered (until six segments of the frequency display are occupied). This is entered from the right and the most significant bit is displayed on the left,

i.e. D_5 D_4 D_3 D_2 D_1 D_0

Pressing the 'STORE' key will cause the data to be set into the appropriate latch; all five decimal points will be displayed briefly to indicate that the data has been accepted.

Note ...

If a read only latch has been selected by mistake Error 13 'Latch write error' will be displayed.

43. 8-bit data. To enter data in this format each bit is assigned a binary weighting according to its position. The sum of all eight bits is taken and entered. Procedure for entering data is as described in the previous paragraph and pressing the 'STORE' key causes the latch to be set.

e.g.

D_0	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
D_1	2	1	0	0	1	1	0	1	1
D_2	4	128	+ 0	+ 0	+16	+ 8	+ 0	+ 2	+ 1
D_3	8								
D_4	16				Enter 155				
D_5	32								
D_6	64								
D_7	128								

44. The l.e.d. latch, IC4 on A1 board may be conveniently used to illustrate the procedure. The latch address is 01, therefore key in the following:-

2ND FUNCT, 3,0,1,1,6,9, STORE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	1	0	0	1
128	+ 0	+32	+ 0	+ 8	+ 0	+ 0	+ 1

The following l.e.d's will then be lit

D_7 2ND FUNCT

D_5 AM

D_3 CARR FREQ

D_0 Δ

45. Second function 3 application. The facility is an invaluable aid when wishing to assess latch serviceability and/or its data outputs. Connect a storage oscilloscope whose trigger input is connected to the address line and monitor the data lines as they reach first the latch inputs, and then the latch outputs. This will show if the latch is operating correctly.

Notes ...

(1) A separate second function control (Second function 6) is available to check the l.c.d. when required therefore A1, IC1, IC2 cannot be written to manually.

(2) Writing arbitrary data to A1, address [00] could lock out the operator. Users with GPIB control however can write to the latch without hindrance.

(3) Writing arbitrary data to addresses [15] - [22] (GPIB write registers) may affect GPIB operation if in use. It is therefore preferable to carry out this operation from the keyboard.

TABLE 5 2022 LATCH ADDRESSES

2ND FUNCT 3 Address No.	Latch description	Location IC No.	Location Board	Circuit diagram reference
00	Keyboard row set	3	A1	44828-781B
01	Front panel l.e.d. driver	4	A1	44828-781B
02	READ keyboard column	5	A1	44828-781B
03	READ interrupts	13	A2	44828-784Z
04	Select modulation function	11	A2	44828-784Z
05	Attenuator pads	22	A2	44828-784Z
06	RF range	25	A2	44828-784Z
07	Fine modulation	19A	A2	44828-784Z
08	Coarse modulation	19B	A2	44828-784Z
09	LF FM extension	20A	A2	44828-784Z
10	FM tracking	20B	A2	44828-784Z
11	Jitter correction	27A	A2	44828-784Z
12	Voltage tuned filters	27B	A2	44828-784Z
13	RF level calibration	24A	A2	44828-784Z
14	RF level	24B	A2	44828-784Z
15	GPIB register WRITE 0	2	AD0	54433-003N
16	1		AD0	54433-003N
17	2		AD0	54433-003N
18	3		AD0	54433-003N
19	4		AD0	54433-003N
20	5		AD0	54433-003N
21	6		AD0	54433-003N
22	7		AD0	54433-003N
23	GPIB register READ 0		AD0	54433-003N
24	1		AD0	54433-003N
25	2		AD0	54433-003N
26	3		AD0	54433-003N
27	4		AD0	54433-003N
28	5		AD0	54433-003N
29		6	AD0	54433-003N
30		7	AD0	54433-003N
31	10 Hz positive increments	23	AA1	44828-786E
32	640 Hz positive increments	24	AA1	44828-786E
33	Mod. control and -2.56 MHz increments	19	AA1	44828-786E
34	10.24 MHz positive increments	13	AA1	44828-786E
35	40 kHz negative increments	3	AA1	44828-786E

46. **Data entry**

- 6-bit addresses 00, 02-06, 31-35 inclusive
- 8-bit addresses 07-30, 01 inclusive
- Read addresses 02, 03, 23-30 inclusive
- Write addresses 00, 01, 04-22, 31-35 inclusive

8-bit data is entered in decimal notation, whilst 6-bit is in binary.

FAULT FINDING TO BOARD LEVEL

47. The following section describes fault finding routines using tables which may be used to help diagnose faults down to board level. The fault finding routines start from a generalized fault condition and guide the operator to the most likely area of the fault. The generalized fault conditions used as a starting point are as follows:

(a) Front panel failure

(b) Output frequency error

(c) Output r.f. level error

(d) RPP failure

(e) AM fault

(f) FM/ΦM fault

(g) Residual noise on carrier frequency

(h) Excessive carrier harmonics

(i) GPIB fault

48. Choose the description that most closely describes the fault condition and use the fault finding guide to establish the area of the fault. Before using the fault finding tables read the accompanying notes. The construction of the instrument is such that it should be possible to locate and correct all faults without resorting to special adapters or extender cables. Where board exchange is practised or where the repair to a board is such that recalibration may afterwards be required, see Instrument calibration section later in this chapter for details.

Front panel failure

49. A chart to aid fault finding in this area is given in Table 6. A front panel failure is defined as a fault in which the keyboard or the information given on the l.c.d. and l.e.d's is abnormal.

50. The fault is likely to be one of three boards or the interconnections between these;

Suspect boards	Interconnections
AA2 Microprocessor	AA2 (PLAC) - A2 (PLL)
A2 Power supply & control	A2 (PLF) - Transformer T1
	A2 (PLH) - A0 power devices TR1, IC1
	A2 (PLK) - A1 (SKK)
A1 Keyboard & display board	A1 (SKK) - A2 (PLK)

Fig. 14 shows the format in which data is transferred between boards and Table 6 should assist in diagnosing which of the three boards is at fault. Generrally information from the microprocessor is transmitted in serial form to A2. Here its format is modified to suit the device being controlled. The l.c.d. drivers use a special format serial link whilst the keyboard and l.e.d's are controlled using a parallel bus.

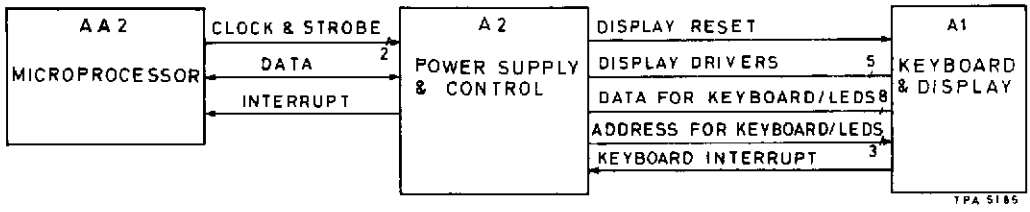


Fig. 14 Data transfer between boards

51. The microprocessor is interrrupt driven, so that key presses need to cause an interrupt before the processor will take data from A2 to check the state of the keyboard. If the microprocessor is serviceable but a fault exists in the memory, then an error number may be displayed depending on the location of the fault. Error numbers are displayed in the carrier frequency window as shown below. Table 7 gives details of all available error numbers.

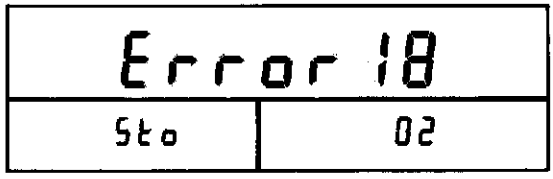
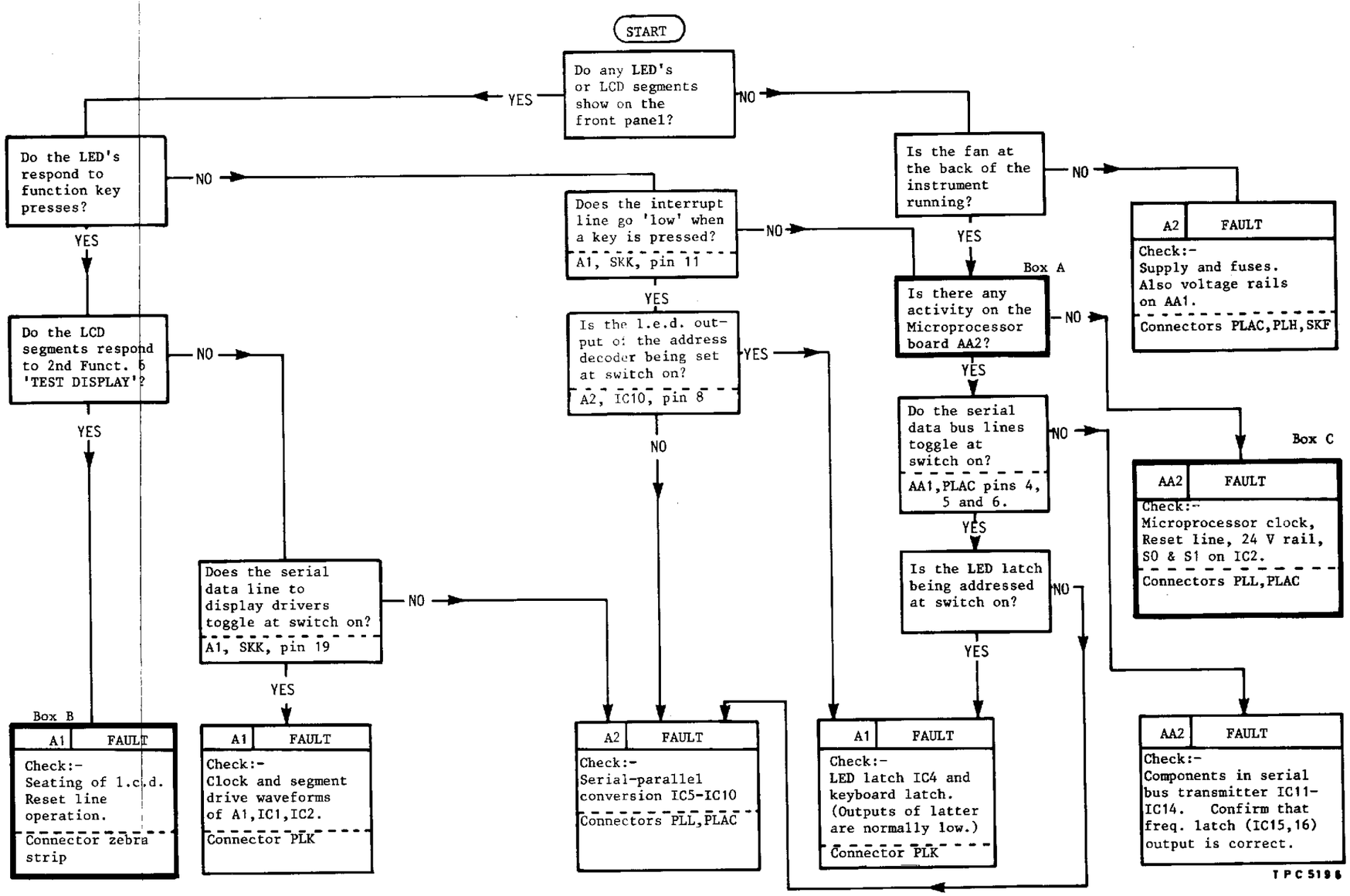


TABLE 6 FRONT PANEL FAILURES



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A1 Keyboard & display board	A1 (SKK) - A2 (PLK)

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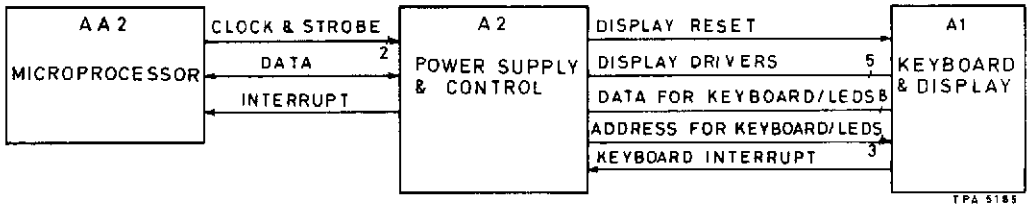

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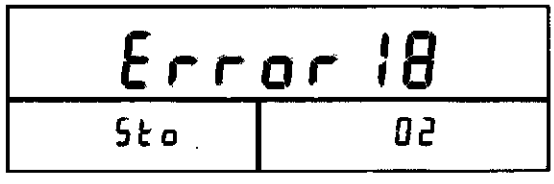


TABLE 6 FRONT PANEL FAILURES

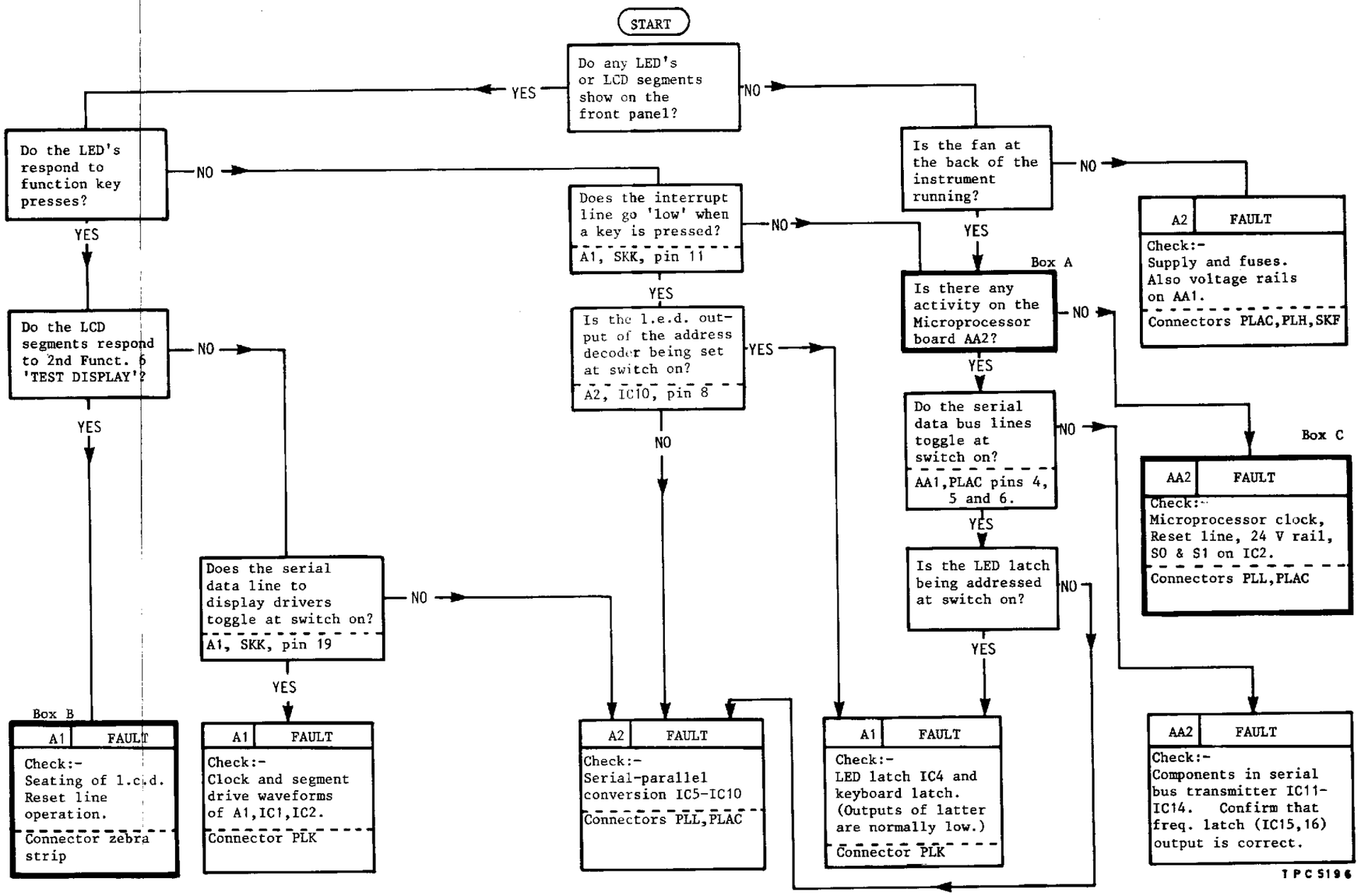


TABLE 7 ERROR MESSAGES (AA2)

Error No.	Error condition
01*	Request outside limits
02*	Incorrect key code sequence
03*	Too many digits
04*	Incorrect unit
05*	RPP trip
06	RAM check failure (IC9)
07	EAROM checksum failure (IC10)
08	EPROM checksum failure (IC5-IC8)
09*	External modulation outside ALC range (LOW)
10*	External modulation outside ALC range (HIGH)
11*	External standard selected but not applied
12	External standard frequency not locking
13	Latch write error
14	EAROM write error
15	EAROM recall error
16	GPIB bus error
17	Unrecognized GPIB mnemonic/character
18	Attempt to write to protected store

* These error numbers refer to GPIB Error conditions and therefore do not indicate on the front panel display.

52. Error 06 RAM check failure. This test is carried out by writing a series of '1's and '0's into the RAM and then reading them back.

Error 07 EAROM checksum failure. This is carried out by summing the calibration data and a checksum byte. If the result is not FF then error 07 will be displayed.

Error 08 EPROM check failure. This is similar to the EAROM check. Data that is stored in memory is also checked. If error 07 is displayed when a store is recalled it indicates that the stored data has been corrupted.

53. Box A (see Table 6) Microprocessor activity. If the display is blank or there is no response from the keyboard, it will be necessary to gain access to AA2 board. At switch on, data to set up all the latches will be sent over the serial bus. The processor will then go into a loop WAITING FOR AN INTERRUPT. Examination of the low order address/data lines from the processor with a logic probe should reveal activity in both cases. Data, clock and strobe lines should be checked immediately after switch on.

54. Box B (Abnormal l.c.d. presentation). If the reset line to the l.c.d. drivers fails to operate it is likely that the left and the right sides of the display will be different in appearance, with the contrast on the right hand side poorer than that on the left hand side.

55. Box C (No microprocessor activity). Although an error number may not be displayed this does not preclude the possibility of either a RAM or an EPROM fault. If the microprocessor is unable to run the system and fails to respond at all, first check for obvious faults e.g. ICs running hot, clock input, (5 MHz at IC2 pin 1) and clock output (2.5 MHz at pin 37).

RESET 'L' on pin 36 (this will be 'low' if +5 V rail falls below +4.5 V) and the Memory protection circuit, (+21 V at test point 13).

56. If no address/data lines are active, check the state of IC2, S_0 pin 29 and S_1, pin 33 advanced timing signals. Because these have no direct application on 2022 they are not shown on the circuit diagram. It is possible that the processor has misinterpreted the address or data lines and as a consequence performs a halt instruction. Confirm this by checking for logic 'low' level on both S_0 and S_1 lines. Table 8 shows the machine cycle status for the states available from which other possible errors can be determined.

TABLE 8 PROCESSOR MACHINE CYCLE STATUS (AA2)

S_0	S_1	States
0	0	Halt
0	1	Memory read
1	0	Memory write
1	1	Op code fetch

Output frequency error

57. Assistance in finding an output frequency error is given in Table 9. An output frequency error is defined as a fault in which the frequency, when measured using a frequency counter operating from the same frequency standard as the instrument, indicates that the output differs from the value set.

58. When the instrument is using an external frequency standard ensure that this is of the correct level, greater than 1 V r.m.s., and the correct frequency, 1,5 or 10 MHz. Check Second function 1 'Status' to determine which of the three is internally selected. Instructions on changing the internal selection, normally set to receive a 10 MHz standard are given in the Re-calibration section of this chapter.

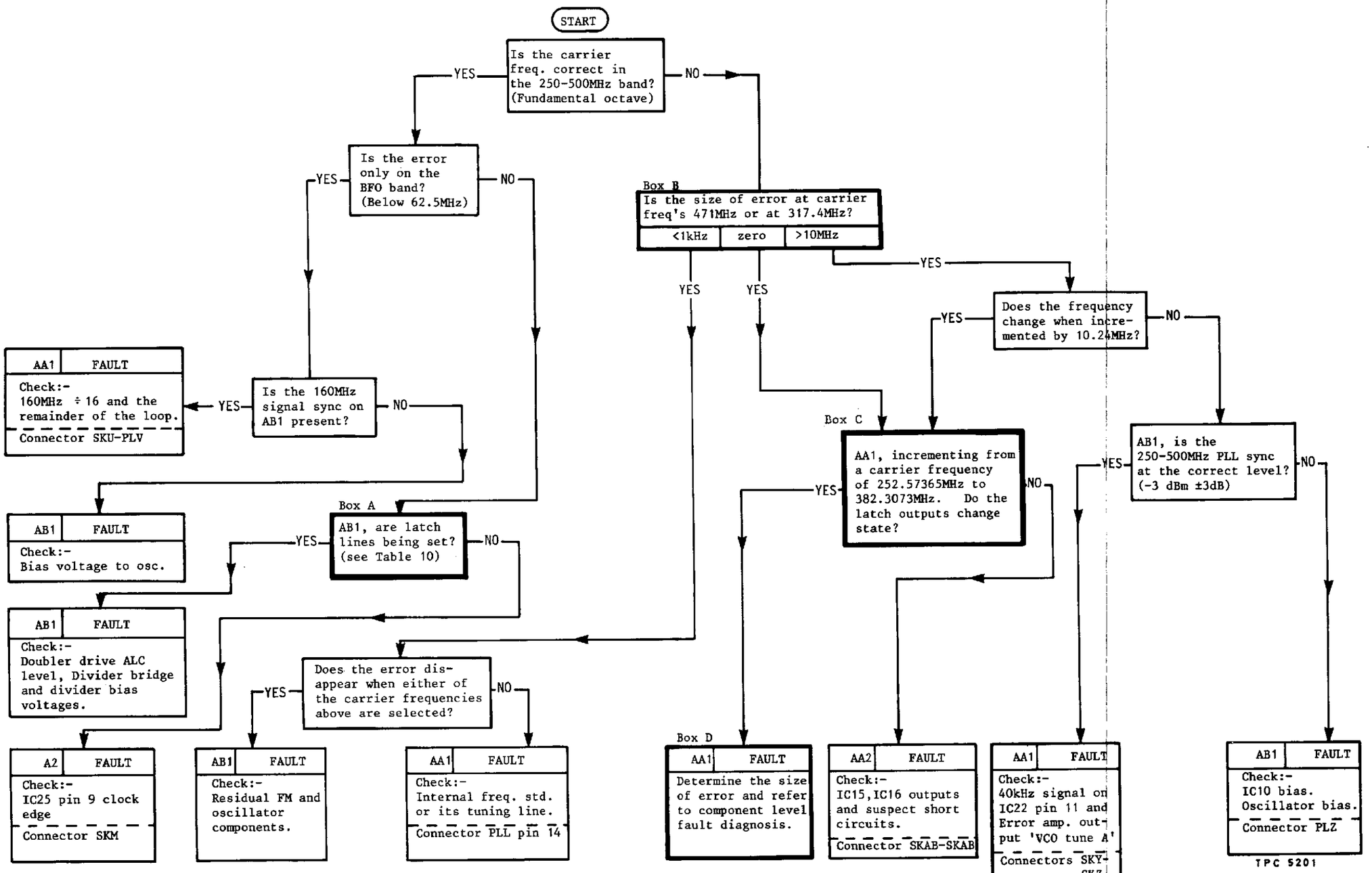
59. The following boards are those that are in some way concerned with the generation of the output frequency and could be in some way at fault.

AA1	Synthesizer
AB1	RF signal processing
A2	Power supply/Control
AA2	Microprocessor

60. Before carrying out extensive tests on a board check the following connectors which could be at fault:

SKV - SKW	160 MHz sync from AB1 to AA1
SKY - SKZ	250-500 MHz sync from AB1 to AA1
PLAB	Microprocessor to synthesizer
PLM - PLAD	A2, Control to AB1

TABLE 9 OUTPUT FREQUENCY ERROR



61. Signal frequency faults can be divided broadly into three categories;

(1) RF signal processing - division, multiplication or mixing

(2) Frequency synthesis

(3) Variations in the reference frequency

Initially it is advisable to begin by checking the fundamental octave 250-500 MHz. If this is not where the fault lies, suspect a category (1) fault.

62. Box A (see Table 9) AB1 control lines. Select and switch between the two carrier frequency settings shown in the table below. Switching between the two should cause all four bits of data to change. If the frequency is not correct on the fundamental band suspect either the synthesizer or reference frequency standard, depending on the size of the error.

TABLE 10 AB1 CONTROL DATA

Selected frequency	A_0 pin 6 (2nd brown lead)	A_1 pin 11 (2nd red lead)	A_2 pin 5 (White lead)	OSC HIGH pin 10 (2nd yellow lead)
10 MHz	0	1	1	0
200 MHz	1	0	0	1

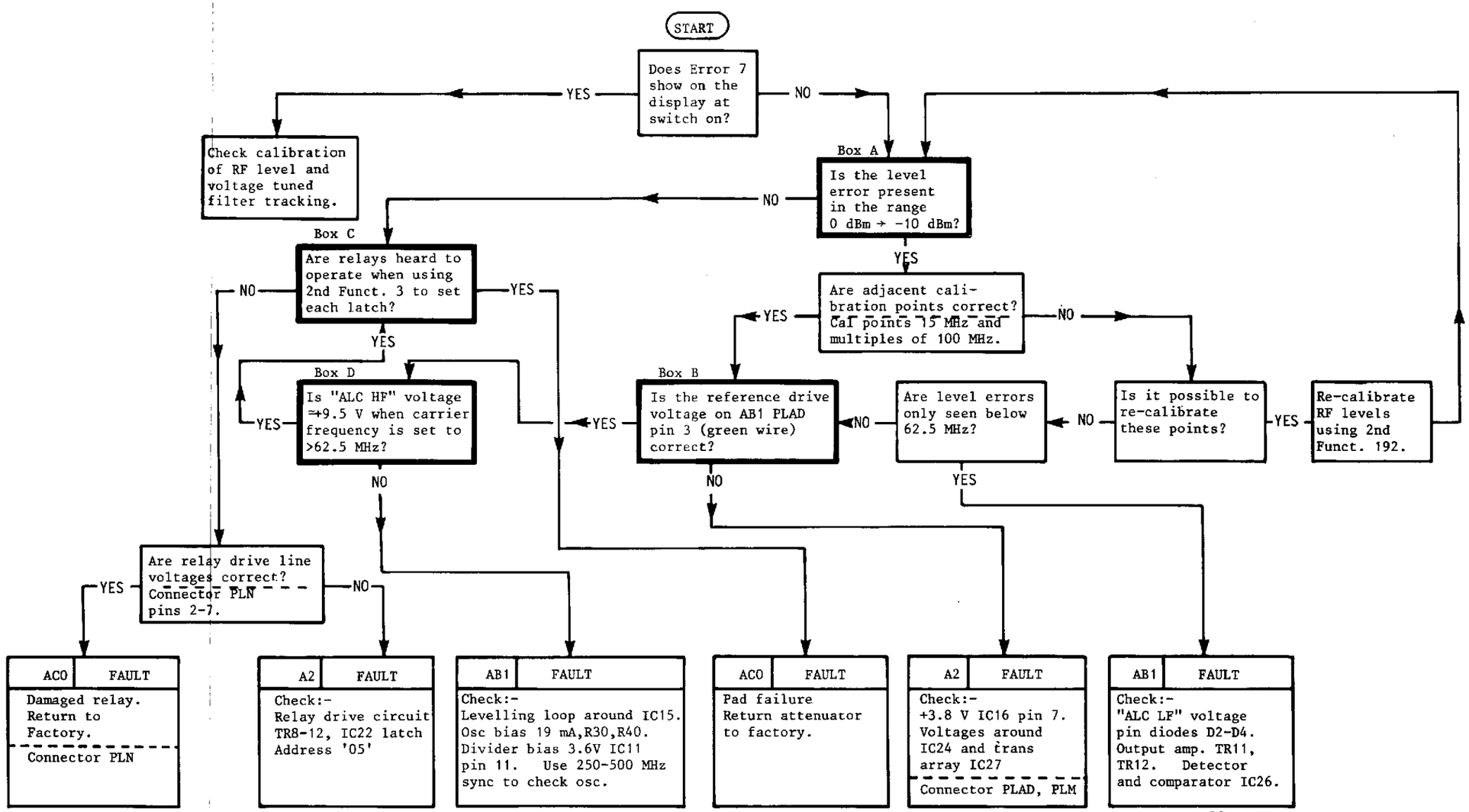
63. Box B (Size of frequency error). With reference to box B, shown in Table 9, two selected frequencies, 471 MHz and 317.4 MHz are called for. These are chosen such that only the four modulus divider IC9 on AA1 is in use. A "zero" error implies an error that is within the drift limit of the internal reference frequency measurement accuracy.

64. Box C (Significant frequencies). The two frequencies chosen here, 252.57365 and 382.3073 MHz cause all of the frequency setting latch outputs to change state. First enter the lowest frequency 252.5736 MHz and then use a 50 Hz positive increment. STORE this in location 02. Now enter 382.30730 MHz and STORE in location 03. If RECALL is now used the increment keys can be used to change rapidly between one setting and the other. The increment up key will require pressing each time RECALL 02 is used to set the last 3 bits in IC23 correctly.

TABLE 11 FREQUENCY LATCH SETTING DATA

Frequency	IC13	IC19	IC3	IC24	IC23
252.57365 MHz	011001	01	010101	010101	010101
382.3073 MHz	100110	10	101010	101010	101010
DATA BIT	D_5 ---- D_0	D_1 ---- D_0	D_5 ---- D_0	D_5 ---- D_0	D_5 ---- D_0

TABLE 12 RF LEVEL ERRORS



RF level errors

65. A chart to aid fault finding in this area is given in Table 12. An r.f. level fault is defined as a failure which results in the r.f. level being out of specification but the carrier frequency is correct. In assessing that the r.f. level is out of specification the r.f. level offset facility (second function 15) should be switched off. It is also assumed that the error is such that the instrument does not simply require re-calibration.

66. If error number 07 (EAROM CHECKSUM FAILURE) is displayed at switch on it is possible that a mistake has occurred during calibration or that data in the non-volatile memory AA2, IC10 has been corrupted, or is not storing data. Usually (but not always) such faults will also be accompanied by f.m. tracking, AM calibration and tuned filter tracking errors.

67. Because the attenuator unit is a possible source of trouble it simplifies fault finding to initially set this to be out of circuit. This may be done by selecting an r.f. level setting of 0 dBm. All of the pad relays will then be de-energized. The fault is likely to be one of three boards or the interconnections between these,

Suspect boards	Interconnections
A2 Power supply and control	A2 (SKM) - AB1 (SKAD)
AB1 RF processing	A2 (SKM) - AB1 (SKAD)
AC1 RF attenuator	SKN - Power supply to AC1
	PLAE - RF signal to AC1
	PLAF - RF signal AC1 to front panel SKB

68. Box A (see Table 12) Attenuator/fine level control errors. If the fault is confined to level selections below -10 dBm it is possible to differentiate between attenuator or fine level control faults by adding multiples of 10 dB to the level. As the level is increased it may become obvious that a gross error is present with a particular pad in circuit. If however the error is present when the attenuator is no longer contributing to the insertion loss the fine level control is suspect.

69. Box B (AB1 Reference drive voltage). Check that, with a carrier frequency of 200 MHz selected, the following nominal voltages are present on AB1, PLAD, pin 3.

RF level setting	Drive voltage
+6 dBm	1.28 V
0 dBm	0.6 V
-6 dBm	0.27 V
-10 dBm	0.15 V

70. Box C (Attenuator relay function). Each of the relays can be selected individually by utilizing the second function 3 mode of operation. Details of this procedure is given in "Use of second function 3 (Manual latch setting). Each relay is accessed by the method described in the RF output paragraphs and Table 3, both found in this chapter.

71. Further use of the second function 3 control can be made to select each relay in turn and enable these to be heard to de-energize and re-energize. Data is set to '1' logic high, then returned to '0' logic low. Press the STORE key after each bit of data is set to '1' or reset to '0'. Begin with D0 - D4 all set to '0', all relays should now be energized. Set each data bit in turn to logic '1', STORE, then reset to '0' and STORE again.

D0 set to '1' de-energizes RLA
D1 set to '1' de-energizes RLB
D2 set to '1' de-energizes RLC
D3 set to '1' de-energizes RLD
D4 set to '1' de-energizes RLE

If the attenuator unit is suspected, remove AB0 unit; the attenuator can then be detached from this without further dismantling by removing the four securing screws and the conhex connector from AB1.

Note ...

When refitting AB0 unit take care to prevent damage to the GPIB board, AD1 if this is fitted.

72. Reverse power failure. A TO5 relay in the attenuator unit (RLF) gives protection for the attenuator's resistive elements by presenting an open circuit to the output connector SKAF if excessive voltages are detected on the signal line. Testing of this circuit is described in the Performance checks. If a fault is suspected, it is safer to set the r.f. level to 0 dBm to give protection to the pads.

73. Should the RPP not trip, check for correct operation of the detectors D1 and D2. This can be achieved by raising the rear of unit AB0 slightly to give access to PLN, see Fig. 13. Set the r.f. level to 0 dBm, then apply +5 V between earth and the centre pin of the output connector. Connect a voltmeter between earth and PLN, pin 9; this should read approximately +0.25 V. Reverse the polarity of the applied voltage. Now apply the voltmeter positive terminal to earth and the negative terminal to PLN, pin 10. The voltage should be approximately -0.25 V.

Note ...

If a very high impedance voltmeter is used it is possible that hum picked up from surrounding connectors will be peak detected. This will give a standing reading of voltage even when a voltage is not applied to the output connector. Either subtract this offset from the reading obtained when carrying out the test or alternately shunt the voltmeter with a 100 kΩ resistor.

74. Most faults are likely to be confined to either AC1 attenuator board or A2 Power supply and control board. The most likely suspect interconnection is PLN, AC0 attenuator to A2 control.

75. Attenuator accuracy. The only electrical adjustment provided on AC1 is a series of flags which may be used to adjust the calibration of each pad. In the 0 dBm attenuation condition the attenuator has an insertion loss which is dependent upon the frequency selected. This insertion loss is compensated for by RF level calibration. The flags are used to adjust the attenuation of each pad so that the difference between the attenuation of each pad being in or out of circuit is equal to the nominal attenuation of the pad at 1 GHz.

76. To carry out comprehensive attenuator accuracy checks and re-alignment requires each pad to be set up separately using specialized measuring facilities. It is therefore recommended that this be carried out only by the nearest Marconi Instruments agent or Service Division. A spectrum analyzer may be used to check levels down to -90 dBm with limited accuracy.

AM faults

77. Two systems are used to achieve the required modulation. The first system employs a fixed frequency modulator when carrier frequencies up to 62.5 MHz are selected. The second system (for carrier frequencies above 62.5 MHz) uses envelope feedback operating around the output amplifier.

78. If the fault is such that the a.m. fails completely it should be possible to locate this by following the a.m. path from the modulation source. If some a.m. is present but with the incorrect depth, check to see which of the two systems described above are defective. It is assumed that it is not possible to carry out the normal re-calibration procedure.

79. The following boards and connectors are possibly connected with an a.m. fault.

Suspect boards		Interconnections	
A2	Modulation control	A2 (PLM)	- AB1 (SKAD)
		A2 (PLJ)	- Front panel (SKA)
AB1	RF signal processing	AB1 (SKAD)	- A2 (PLM)
AA1	Internal mod. source	AA1 (PLT)	- A2 (PLL)

80. Box A (see Table 13) 160 MHz amplitude modulator fault. Select a carrier frequency of 15 MHz, modulation depth of 80% and an r.f. level of 0 dBm. Check at AB1, PLAD, pin 5 (white wire) for a sinewave with a zero mean and peak amplitude of 5.5 V.

Note ...

When AB1 unit is disconnected from A2 board there is a slight loading effect on the voltage seen on A2, approximately 0.5 V.

81. Box B (Envelope feedback fault). Envelope distortion may occur if there is a restriction on the level range. Using the internal modulation output as a sync signal it should be possible to determine whether the peak power is limited. AM is applied in the same sense as the voltage on the MOD IN/OUT socket, where a positive voltage means a greater power level.

82. Box C (Square law correction error). If the trough of the modulation envelope is at fault it is possible that the square law correction circuit on A2 board is malfunctioning. A further possible cause is a severe leakage to earth on AB1 board. Check the voltage on AB1, PLAD, pin 3 (green wire) this should fall to 0 V, or slightly negative depending on the setting of the Detector correction potentiometer A2, R90.

TABLE 13 AM DEPTH ERRORS

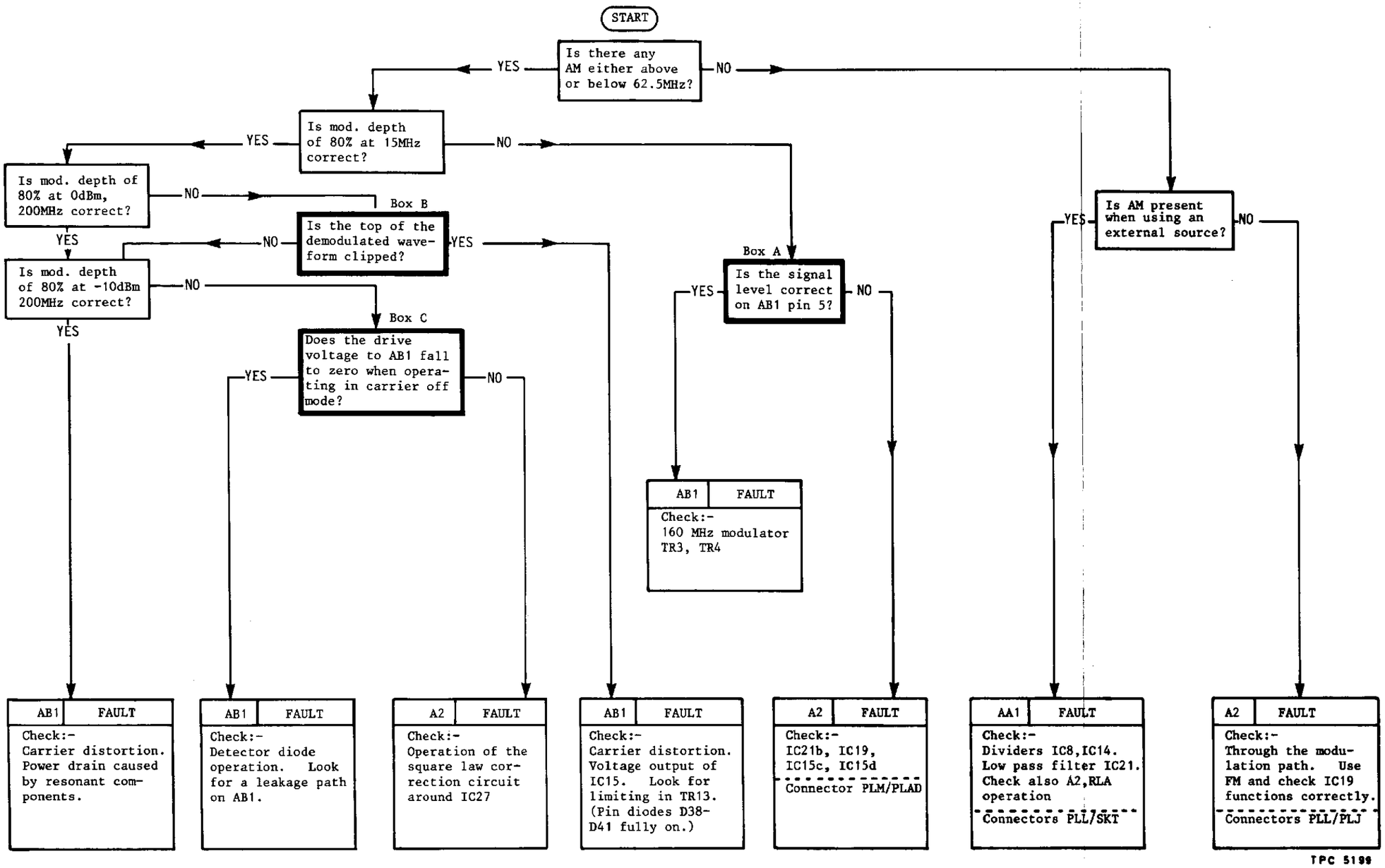
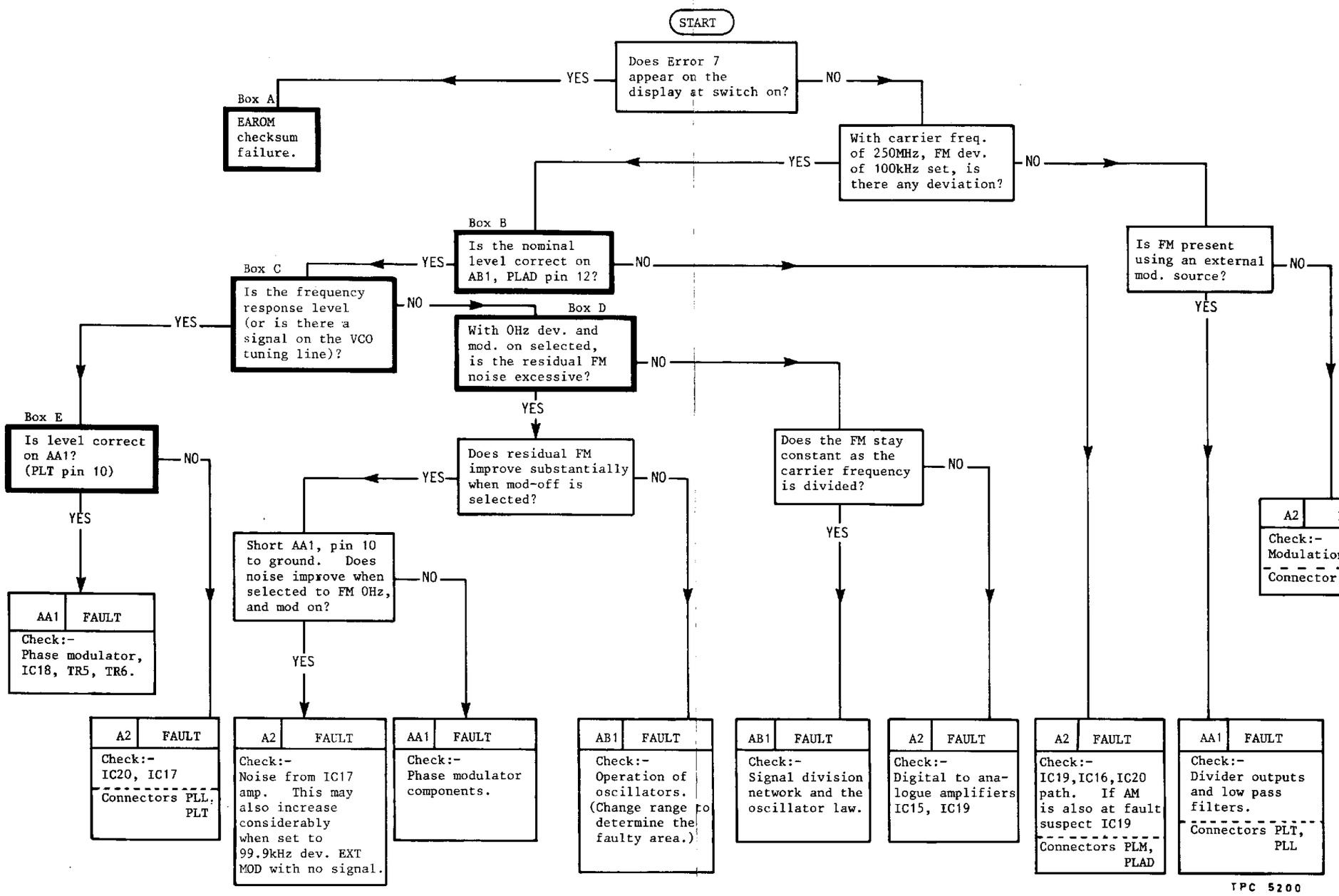


TABLE 14 FM DEVIATION ERRORS



FM and ΦM faults

83. An f.m. fault finding guide is given in Table 14, it is assumed that the fault cannot be rectified by simply re-calibrating the instrument. Frequency modulation at rates greater than 1 kHz is mainly derived by simply applying the signal to the v.c.o. tuning line. A differentiator in the signal path creates phase modulation (6 dB/octave pre-emphasis). The deviation that is applied over the fundamental octave is scaled appropriately for the doubler and divider bands.

84. Angle modulation at low frequencies is achieved by introducing a phase modulator into the reference signal path of the synthesizer. By intergrating the signal driving the phase modulator an equivalent of frequency modulation is then obtained.

85. The following boards and connectors are possibly connected with an f.m. or ϕ.m. fault:-

Suspect boards	Interconnections
A2 Modulation control	A2 (PLM) - AB1 (SKAD) Signal from mod. control
AA1 Low freq. modulation source	A2 (PLL) - AA1 (PLT) Mod. signal from AA1 to A2
AB1 FM and VCO drive	A2 (PLJ) - Modulation in/out

86. Box A (see Table 14) Error 7, EAROM checksum error. First check that the reason for this display is not operator error (EAROM checksum not reset via 2ND FUNCT 195 after re-calibration procedures). Information on the resetting of the EAROM checksum, if required is given in the Re-calibration Section of this chapter. Assuming that a fault is present it is most likely to be caused by corruption of data for some reason. As an aid to diagnosing a fault in the f.m. tracking store Table 15 gives a list of carrier frequencies used as f.m. tracking points together with the typical values of f.m. tracking data. Normally instruments will be within approximately 20% of the values listed below. There should be no abrupt changes in value except possibly where the oscillator ranges change over at 353 MHz.

87. In the course of fault finding if it is required to check the input and output levels of the various digital-to-analogue converters this can best be carried out using a digital a.c. voltmeter and 2ND FUNCT 3 mode to access each IC as required. The latch address numbers are given both in Chap. 7 Servicing diagrams and in Table 5 of this chapter.

88. Box B (FM level). Set the carrier frequency to 250 MHz, FM 99.9 kHz. Use 2ND FUNCT 3 to set address 10 to '200'. Check that the signal on AB1, PLAD, pin 12 (black wire) is 5.2 V p-p.

TABLE 15 TYPICAL FM TRACKING DATA

OSC 1		OSC 2	
Frequency	Data	Frequency	Data
250 MHz	194	353 MHz	125
254.12	204	358.88	132
258.24	212	364.76	137
262.36	218	370.64	141
266.48	221	376.52	143
270.60	223	382.40	144
274.72	223	388.28	144
278.84	222	394.16	143
282.96	219	400.04	141
287.08	215	405.92	139
291.20	211	411.80	136
295.32	207	417.68	133
299.44	202	423.56	130
303.56	197	429.44	128
307.68	193	435.32	125
311.80	189	441.20	123
315.92	186	447.08	121
320.04	184	452.96	120
324.16	182	458.84	119
328.28	181	464.72	118
332.40	180	470.60	118
336.52	180	476.48	119
340.64	182	482.36	120
344.76	183	488.24	122
348.88	185	494.12	124
352.9999	189	499.9999	127

89. Box C (Frequency response). Apply an external modulation of 1 V r.m.s. at a frequency first of 1 kHz and then at 100 Hz. If there is a marked difference in the frequency response between the two then suspect the low frequency modulation path. An alternative method of checking the reference phase modulator is to examine the a.c. signal on the v.c.o. tuning line AB1, PLAD, pin 16 (red wire). If the f.m. tracking is set correctly there should be less than 5 mV p-p of the 1 kHz signal.

Note ...

The 1 kHz MOD IN/OUT output from 2022 can be used to synchronize an oscilloscope enabling the above to be seen more easily.

90. Box D (Excessive residual f.m.). If excessive f.m. is present on the carrier frequency a higher than normal deviation can be expected. To check for residual noise set 0 Hz, FM and monitor the output of a low noise modulation meter (2305) set to measure f.m. If noise is excessive follow the additional procedures given in Table 14, and para. 92.

91. Box E (LF FM level fault). Select a carrier frequency of 250 MHz and a deviation of 99.9 kHz. Check at AA1, PLT, pin 10 (black wire) for a 1 kHz, 150 mV p-p signal.

92. Box D (Residual noise on carrier frequency). If excessive noise is present on the carrier frequency several possible sources must be considered. Initially check to assertain which of the following is the problem source then carry out the necessary remedial action.

(1) AM noise (carrier frequencies above 62.5 MHz). Due to the action of the levelling loops it is unlikely that changes in amplitude of signals prior to the output amplifier will be transferred to the final signal. If it is found that the correction voltage on AB1 test point "ALC HF" (junction of IC15 pin 6 and R112) is noisy this is likely to be caused by disturbances on the reference level line. Use an oscilloscope to check the signal on AB1, PLAD, pin 3 (green wire). With no AM applied it should be a d.c. level free from fluctuations. If not suspect the modulation control circuit on A2 board. To access this remove unit AB0 and retrace the modulation path from A2, PLM, pin 3.

(2) AM noise (carrier frequencies below 62.5 MHz). The response of the levelling loop is extremely slow on this frequency range and because of this noise on the reference line AB1, PLAD, pin 3 (green wire) will have less effect than noise on the AM drive line AB1, PLAD, pin 5 (white wire). Check this for any fluctuations and retrace these to A2 board if necessary.

(3) FM noise. Check to establish first that the fault is common to carrier frequency selections of both above and below 62.5 MHz or confined to one range only. Ensure that the measuring instrument is not at fault.

Below 62.5 MHz only. Here the 160 MHz loop is suspect. If the frequency of the disturbance is comparatively high (above several hundred hertz), check AB1, 160 MHz v.c.o. circuit particularly around TR1. Scintillation in the capacitors can cause an audio crackling noise. This can be checked by monitoring the 2305 l.f. output with a loudspeaker.

Above and below 62.5 MHz. With noise in this category it will be necessary to determine whether oscillators or the control signal is at fault. Selecting carrier frequencies of 352 and 354 MHz respectively will change from one oscillator to the other. This will indicate a fault on one or the other oscillator unit if either of these are faulty. Use of the MOD ON-OFF selection will switch AA1 phase modulator on and off. If the f.m. is set to 0 Hz, this is the next most likely cause. Also check AA1, PLT, pin 10 (black wire) LF FM line. To check the performance of the modulator signal path select EXT MOD and a deviation of 99.9 kHz. If the noise increases use Second function 3 to control the gain of A2, IC20, (address 09 and 10), A2, IC11, (address 04) and A2, IC19 (address 07 and 08) until the noise level drops. The cause should then be apparent.

Note ...

Other inadequately screened instruments radiating magnetic fields at the line frequency can also be the cause of excessive hum components. If noise is present on both oscillators with the f.m. modulation off and there is no apparent noise on the FM line A2, PLM, pin 12 (black

wire) - look for 100 µV or less (in the 50 Hz - 50 kHz bandwidth), suspect the loop error amplifier if this is excessive. Check the noise on the VCO TUNE A line at A2, SKM, pin 16 (red wire); this should be approximately 1 mV p-p. Measurement bandwidth is unimportant in this case.

Excessive carrier harmonics

93. If the harmonics are found to be in excess of the specification suspect AB1, RF processing board. Check the instrument and establish which carrier frequency range is at fault then carry out the remedial action suggested below.

94. Carrier frequencies up to 62.5 MHz. The harmonic level for these frequencies are determined by three factors:-

(1) The performance of fixed filters made up of printed circuit inductors and ceramic plate capacitors.

(2) The drive levels to the mixer that creates the b.f.o. signal.

(3) The linearity of the b.f.o. output amplifier. Of the three, (2) or (3) are most likely to be the cause of the problem.

95. Basic operation of the mixer drive may be checked by measuring the voltages on the two following test points:-

AB1, 'ALC DOUBLER' (adjacent to IC12a), should be 4 V ±0.25 V.
'ALC LF' (adjacent to R13) with a 50 Ω load connected should be as follows:-

6.5 V - 7.5 V at a level of -10 dBm and
6 V - 7 V at a level of 0 dBm

Notes ...

(1) When monitoring the 'ALC DOUBLER' voltage, some variation of voltage will be observed across the frequency band.

(2) Poor alignment of the LF AM MOD tuning capacitor C18 may also be a cause of a voltage abnormality on the 'ALC LF' test point.

96. Fault finding on the two stage output amplifier should be simple with each stage being independently biased. R65 is present to prevent ultra high frequency oscillations which would otherwise give misleading results. Voltages expected at TR11 collector, +6 V, and TR12 collector, +4.8 V. C94 may be disconnected if required allowing for the injection of a test signal to be applied through the amplifier.

97. Carrier frequencies from 62.5 MHz to 250 MHz. The factors that influence the harmonic content for this frequency range are the following:-

(1) Signal divider output balance

(2) Fixed LC filters

(3) Linearity of output amplifiers

Of the three (1) or (3) are the most likely cause of the problem. The second harmonic performance for the half octaves 62.5 MHz - 88.25 MHz and 125 MHz - 176 MHz are determined by the balancing of the Q and $\overline{Q}$ outputs of AB1, IC11. The signal quality may be checked before reaching the output amplifier by connecting a 500 Ω oscilloscope probe across C60.

98. A self biasing arrangement, designed to maintain maximum sensitivity of the divider, should result in a voltage of approximately +3.6 V on AB1, IC11, pins 6 and 11. The output amplifier levelling loop should be +9.5 V - +10 V at 0 dBm with a 50 Ω load connected. AB1, IC14, pin 1 should be approximately +3 V. (Note that D42 and D50 are matched devices). A test signal can be injected by disconnecting one side of C102 at the junction of R92. Apply the signal to C102, this should be a.c. coupled and at a level of 0 dBm.

99. Carrier frequencies from 250 MHz - 500 MHz. This frequency range is derived from the fundamental oscillators and uses a combination of a tracking notch filter and a fixed low-pass filter. Generally the second harmonic that reaches the output amplifier is low enough so that the amplifier distortion is what is actually seen at the output. The notch provides cover for the half octave 250 - 353 MHz. Use is made of the same data as that obtained for the band pass filter. To ensure correct tracking L13 (wire loop) is mechanically adjusted to cancel the second harmonic at 250 MHz. If the output amplifier is suspected carry out the checks given in the previous paragraph.

100. Carrier frequencies from 500 - 1000 MHz. This doubler range uses a voltage tuned band-pass filter to reject unwanted components. No mechanical adjustment exists for this filter, it relies on the approximate tracking of D34 - D37 varactor diodes although this tracking is not critical. The drive voltage is obtained by interpolating between points that are found by looking for the minimum insertion loss of the filter. The table below gives an approximation of the voltage that should be present on AB1, PLAD, pin 15 (yellow wire).

TABLE 16 TYPICAL CALIBRATION DATA AND DRIVE VOLTAGES FOR AB1 BAND-PASS FILTER

Carrier frequency	Drive voltage (AB1, PLAD, pin 15)	Calibration data
500 MHz (250)	5.5 V	60
600 (300)	9.0 V	100
700 (350)	11.5 V	120
800 (400)	14 V	150
900 (450)	18 V	190
1000 (499.9)	23.5 V	250

Note ...

At higher power levels (above 0 dBm) where the harmonic distortion may rise above -30 dBc, the output level may be affected due to the peak detecting used to level the signal. This will not normally be significant but unexpected changes of level will result if additional capacitive loading is applied, especially to the output pin of IC14.

GPIB faults

101. Few checks are necessary on this board apart from the clock waveform on IC1 pin 8. The frequency here (although not critical) should be typically 1.2 MHz. If there is no response from the instrument to a GPIB command first ensure that the address that data is sent to corresponds to that held by the instrument. Second function 2 may be used for this. Also check the 'INT REQ' line on AD1. This should change from 'LO' to 'HI' temporarily when the instrument is addressed.

102. If the instrument acknowledges the presence of the board AD1, and it is possible to change the address it is likely that IC2 is serviceable.

103. To check that data is transferred from the GPIB cable to IC2 use a logic probe to check that all data lines toggle when different data is sent over the bus. IC2 pin 26 will be 'low' whilst waiting for data.

FAULT FINDING TO COMPONENT LEVEL

104. Assuming that the fault finding tables have been used to localize a fault, it is likely that the general location will be known. This section therefore gives guidance to allow individual component failures to be located. Information on each of the boards is given as follows:-

105. A1 Display and keyboard

Keyboard - Row set latch, column read buffer
LED displays - Driver latch
LCD - Voltage references, l.c.d. drivers, Latch addresses.

106. A2 Power supply and control

Power supplies - +5 V, +12 V, -12 V, +24 V
Modulation - ALC, mod. control, r.f. level/square law correction
Serial - parallel conversion
Interrupt control
Filter tuning drive
Jitter correction drive
Attenuation drive and reverse power sensing
Latch addresses, A2.

107. AA1 Synthesizer

160 MHz loop
Internal/External standard locking
Internal mod. source - Divider and filter
Synthesizer frequency errors
250 - 500 MHz loop - Four modulus divider, presettable divider, fractional N and correction
40 kHz Phase detector and error amplifier
Phase modulator.

108. AA2 Microprocessor

+21 V EAROM supply
Parallel-serial conversion
Synthesizer drive latches
Clock divider
Microprocessor system.

109. AB1 RF processing board

160 MHz oscillator
160 MHz modulator
BFO mixer
BFO output amplifier and levelling loop
250-500 MHz oscillators
Signal dividers (two stage)
Mixer driver/doubler drive and levelling loop
Signal doubler and band-pass filter
62.5-1000 MHz output amplifier and levelling loop
Control logic states.

Display and keyboard (A1)

110. Row latch IC3. A positive-going transition on IC3, pin 9 will cause data present on inputs D_0-D_5, to be transferred to outputs Q_0-Q_5. Outputs will normally be logic 'low'. Use second function 3 and a storage oscilloscope to monitor the operation.

111. Column read buffer IC5. When a key is pressed the output of that particular column line will go to logic 'high' for approximately 1.5 ms every 6 ms. The column input should remain 'low' for the duration of the key press after the initial key search is complete.

112. LCD reference voltages and driver waveforms. LCD references voltages are generated by TR1 - and should be as follows:-

TR1 collector +0.8 V	All l.c.d. segments may appear on if
R6,R7 junction +2.9 V	these voltages are low.

The l.c.d. driver waveforms, a nominal 130 - 150 kHz square wave can be checked on the lower end of R8. Once display initializing is complete the reset line should be set at logic 'high'. Short circuiting this line to earth will blank the display.

113. Backplane drive waveforms can be conveniently checked with reference to Fig. 15. The amplitude of the backplane segment waveform is determined by the setting of R2 'SET LCD OFF VOLTAGE'. The period of the square waves should be either 12.5 or 25 ms and the combination of their frequency and phase with respect to the backplane determines the state of the display. See Chapter 4 Technical Description for further details.

Note ...

The sequence of data that has to be sent to IC1, IC2 is quite complex therefore it is not practicable to drive the board from other than the instrument's own microprocessor and control circuit.

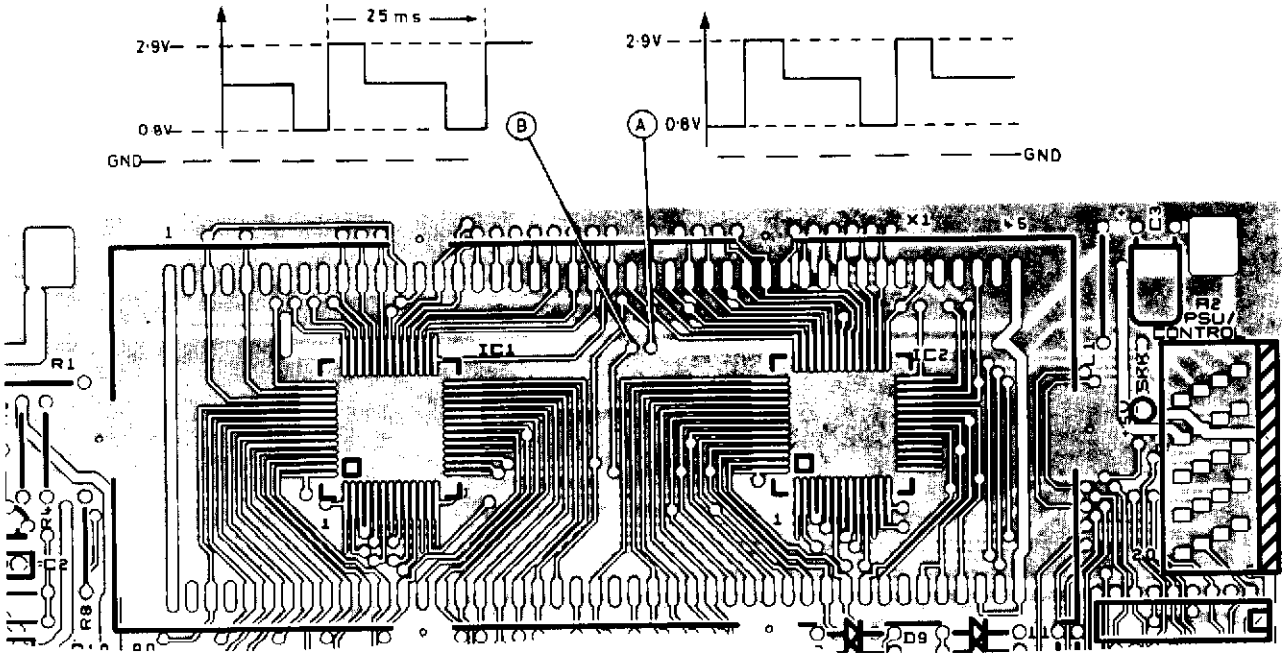


Fig. 15 Backplane drive waveforms and test locations

114. Should there be intermittent contacts, segments of the display will sometimes disappear. If this happens remove the bezel and display, then carefully clean the tin oxide fingers on the l.c.d. and also the solder fingers on the p.c.b., avoid handling the l.c.d. connections and ensure that no solvents come into contact with the polariser on the front of the display.

115. Display and keyboard latch address data. Control data A1. The control data for A1 is shown in the table below.

TABLE 17 DISPLAY AND KEYBOARD LATCH ADDRESS DATA

Address Number	Description	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
00 IC3	Keyboard Row setting	Δ, AM, 8, 3, INT/EXT, RETURN	STORE, RF LEVEL, 5, −, +, MOD ON-OFF	RECALL, 7, 2, MHz, V, TOTAL Δ	MOD ALC, 4, ., kHz, mV, ↓,	CARR FREQ, 1, 9, Hz, μV, 2ND FUNCT	FM,ϕM, 0, 6, % rad dB, CARR ON-OFF,	X	X
	Outputs	Pin 2	Pin 5	Pin 7	Pin 10	Pin 12	Pin 15		
01 IC4	LED driver	Δ	RECALL	MOD ALC	CARR FREQ	FM/ϕM	AM	RF LEVEL	2ND FUNCT
	Outputs	Pin 2	Pin 5	Pin 6	Pin 9	Pin 12	Pin 15	Pin 16	Pin 19
02 IC5	Column Read								
	Outputs	Pin 3	Pin 5	Pin 7	Pin 9	Pin 11	Pin 13	X	X

Power supplies, Modulation control and Data conversion (A2)

116. Check that the following supplies are present

+5 V supply - Requires ±12 V supplies to operate
Collector AOT1 - 10 - 11 V (with no loads)
IC3 pin 7 - +11.5 V
IC3 pin 1 - +6.25 V (with no loads)
R12,R13 junction - +5 V

±12V supplies - These have an internal reference of approximately 1.25 V which can be measured between the ADJ and V OUT pins.
C9 +ve - +10.75 V
C7 -ve - -10.75 V

+24 V supply - Uses a capacitive doubler
C6 +ve - +50 V
C8 +ve - +22.8 V

117. Modulation ALC. TR7 acts as a voltage dependant resistor which changes the gain of non-inverting stage IC15a. IC15b is an error amplifier. IC18a,b, are out of limit comparators. Select 99.9 kHz FM, EXT. Apply 1 V r.m.s., 1 kHz to the MOD IN/OUT socket and select MOD ALC, OFF. The following voltages should then be checked:-

IC15a pin 5 - 2.8 V p-p
IC15a pin 7 - 10 V p-p
D14 cathode - +4.2 V

IC15 pin 8 - -6 V
IC18 pin 7 - -2.4 V
TR7 drain - -0.56 p-p

Select MOD ALC ON, and, using a 10 MΩ probe, check at D14 cathode for 20 mV p-p ripple at 1 kHz. IC15 pin 8, typically -3.5 V will vary depending on the performance of TR7. When voltage goes negative, the stage gain of IC15a reduces.

118. Modulation control path. Three dual, digital-to-analogue converters are used here, IC19,IC20 and IC24. Select CARR FREQ, 200 MHz, FM INT, 99.9 kHz. Using 2ND FUNCT 3 enter 200 into latch address 10 and check the following voltages.

IC15 pin 1 - 7.8 V p-p
IC15 pin 14 - 3.7 V p-p
IC16 pin 8 - 6.6 V p-p
IC17 pin 7 - 4.5 V p-p
IC17 pin 1 - 190 mV p-p
IC21 pin 1 - 5.1 V p-p (short circuit pin 3 to ground)

Using 2ND FUNCT 3 again, enter 1000001 into latch address 04. This brings IC16a differentiator into circuit, the voltage at IC16a pin 8 should not change but there may be high frequency noise on the signal. This will confirm the correct operation of the angle modulation path.

119. RF level/a.m. signal path. With no modulation selected set latch address 13 to 100 and latch 14 to 200 then check the following voltages:-

IC16 pin 7 - +3.8 V
IC21 pin 7 - 0 V
IC16 pin 14 - +1.5 V
IC16 pin 1 - +1.75 V
IC27 pin 13 - +1.1 V
IC27 pin 10 - +1.08 V

The voltage on PLM pin 3 will be that derived on IC27 pin 10 and divided down by R91/R92 and assumes that AB1 is not connected. If it is, then a further drop in voltage can be expected due to the additional loading. Set latch 14 to 10 and check that IC16 pin 1 is +0.625 V and IC27 pin 10 is +40 mV.

120. If the square law correction circuit around IC27 is operating, set latch 13 to 10. The voltage at IC27 pin 10 will be less than 1/20th of the reading than with the latch set to 200 as shown in Fig. 16.

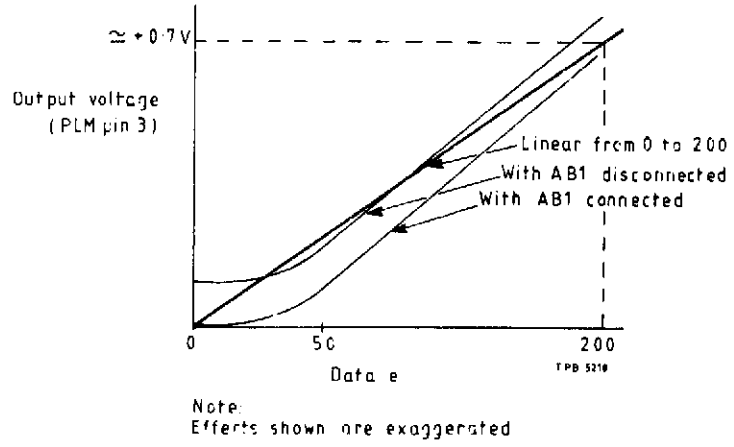


Fig. 16 Effect of square-law correction circuit A2

121. Select CARR FREQ 10 MHz, INT MOD 80%, RF LEVEL 0 dBm. Enter 200 into latch address 07 and check the following a.c. voltages.

IC14 pin 4	-	4.8 V p-p
IC16 pin 7	-	6.4 V p-p
IC21 pin 7	-	11.5 V p-p
IC16 pin 14	-	1.9 V p-p
IC27 pin 10	-	1.6 V p-p

If the waveform at PLM pin 3 is seen to be distorted when applying higher percentages of a.m. at a level of -10 dBm, this effectively confirms the operation of the square law correction circuit and is quite normal.

122. Serial to parallel conversion. Description of the data format and how it is transmitted over the serial bus is described in Chapter 4 Technical Description. However it may not be practicable to monitor the data flow directly unless a fast storage system is available.

123. The most convenient way to check individual shift registers is to look for changes of state on the outputs corresponding to data being clocked in and strobed. Since any key press will require the interrogation of the keyboard by AA2 microprocessor, it should be apparent that activity exists. IC5,IC7 and IC9 control the serial to parallel conversion while IC10 decodes 4 address lines to provide chip enables for individual latches. The outputs of this are normally logic 'high' level.

124. When any key is pressed a 10 µs pulse should be seen on IC4c, when function keys are pressed, pulses should also be seen on IC6 pin 3 and IC8 pin 3.

125. Interrupt control. Pressing a key should cause an interrupt on the RST 7.5 INTERRUPT line of AA2, PLAC, pin 3 and also the following activity on A2.

IC6 pin 12 - Normally 'high' going 'low' for the duration of the key press
IC6 pin 11 - (AND gate) goes 'low'
IC12 pin 11 - goes 'high'

The remainder of IC12 is used to control the routeing for other interrupts. Pins 1 and 2 are normally 'high', pin 1 going 'low' if EXT MOD, ALC ON is selected but with no modulation source applied. IC12 pin 3 then goes 'high' and pin 4 'low', pin 6 should also have been set to 'high' via IC11 pin 10. The RPP TRIPPED line should be 'high' allowing IC12 pin 10 to go 'high'. This is inverted and fed to IC12 pin 13.

126. Filter tuning drive. IC23B controls the d.c. level on TR13 collector. Enter data into latch address 12. Output voltage should increase linearly with data magnitude and reach +23 V at least (possibly before the maximum data point 255 is reached).

127. Jitter correction voltage. The voltage on IC17 pin 8 should vary inversely with frequency. Set CARR FREQ 250 MHz, check the voltage at IC17 pin 8, this should read approximately -4 V. The voltage should decrease in magnitude as the carrier frequency is decreased until at 499 MHz the voltage is approximately -2 V.

128. Attenuator drive and Reverse power sensing. The following checks may be carried out with the attenuator unit out of circuit. IC22 outputs should go 'low' (<1 V) providing the base current for transistors TR8 - TR12, the collectors should rise to almost the supply rail (+5 V). IC18c and IC18d acting as comparators compare the voltages on pins 10 and 13 with those on pin 9 (+40 mV) and pin 12 (-40 mV). Outputs will normally be low (-10.5 V). Application of a voltage above or below ±40 mV should turn TR16 off and the voltage on R103 should then fall from virtually +5 V to 0 V.

Power supply/Control latch address data

129. Control data A2. The control data for A2 is shown in the table below.

TABLE 18 POWER SUPPLY/CONTROL LATCH ADDRESS DATA

Address Number	Description	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
03 IC13	Interrupt READ	MOD LEVEL LOW	MOD LEVEL HIGH	RPP	KEYBOARD	GPIB	CHECK IC11 PIN 10	X	X
	Outputs	Pin 3	Pin 5	Pin 7	Pin 9	Pin 1	Pin 13		
04 IC11	Function setting	INT MOD	AM ON	MOD ALC OFF	INTERRUPT ENABLE	FM >10 kHz	ΦM ON	X	X
	Outputs	Pin 2	Pin 5	Pin 7	Pin 10	Pin 12	Pin 15		

TABLE 18 POWER SUPPLY/CONTROL LATCH ADDRESS DATA (continued)

Address Number	Description	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
05 IC22	Attenuator Drive						RPP RESET		
	0 dB	1	1	1	1	1			
	10 dB	1	1	1	0	1			
	20 dB	1	0	1	1	1			
	30 dB	1	1	1	1	0			
	40 dB	1	1	1	0	0	A 'LOW'		
	50 dB	1	0	1	1	0	TO 'HIGH'		
	60 dB	0	1	1	1	0	TRANSITION		
	70 dB	0	1	1	0	0	WILL RSET		
	80 dB	0	0	1	1	0	THE RPP		
	90 dB	0	1	0	1	0			
	100 dB	0	1	0	0	0			
	110 dB	0	0	0	1	0		X	X
	120 dB	0	0	0	0	0			
	Outputs	Pin 2	Pin 5	Pin 7	Pin 10	Pin 12	Pin 15		
06 IC25	RF control, and LCD reset					LCD RESET	X	X	X
	10 kHz-16.5 MHz	0	1	1	0				
	16.5-62.5 MHz	0	1	1	1				
	62.5-88.25 MHz	0	0	0	0	A 'HIGH'			
	88.25-125 MHz	0	0	0	1	LEVEL			
	125-176.5 MHz	1	0	0	0	WILL			
	176.5-250 MHz	1	0	0	1	BLANK			
	250-353 MHz	1	1	0	0	THE			
	353-500 MHz	1	1	0	1	DISPLAY			
	500-706 MHz	0	1	0	0				
	706-1000 MHz	0	1	0	1				
	Outputs	Pin 2	Pin 5	Pin 7	Pin 10	Pin 12			

07 IC19(A)	Modulation level control AM FM Deviation 0 - 249 250 - 499 500 - 999	Is loaded with a calibration value of data A number proportional to the peak deviation requested is entered Deviation Deviation ÷2 Deviation ÷5
08 IC19(B)	Modulation level control AM FM deviation	Is loaded with a number equal to twice the depth requested (to the nearest 0.5%) Deviation (0 - 999) - setting of 07 latch

	0 - 249	250 - 499	500 - 999
10 kHz-62.5 MHz	6	12	30
62.5-125 MHz	12	24	60
125-250 MHz	24	48	120
250-500 MHz	48	96	240
500-1000 MHz	24	48	120

09 IC20(A)	LF FM extension	Loaded with the eight most significant bits of the synthesizer frequency (when expressed as a binary number).
10 IC20(B)	FM calibration	Loaded with calibration data that is used to track the FM sensitivity curves of the oscillators. See Table 15.
11 IC27(B)	Jitter correction	Loaded with the eight most significant bits of the synthesizer frequency (when expressed as a binary number).
12 IC27(B)	Filter tracking	Loaded with data interpolated from calibration points to tune the band-pass filter and notch filter. Data ranges typically from 60 to 250.
13 IC24(A)	RF level calibration	Entered with data interpolated from calibration points across the band, for a given frequency the value entered is doubled when the output level is above +1.1 dBm.
14 IC24(B)	RF level	RF level in mV is entered. Above +1.1 dBm the value is halved before entry.

Frequency synthesizer and internal modulation sourse (AA1)

130. 160 MHz loop. Check that a 160 MHz signal is present at the junction of R2/C1. A signal within the range -20 dBm to 0 dBm should be sufficient to ensure correct divider operation, a greater or lesser signal will be likely to produce a fault condition. Expected voltages of this stage and the timing sequence of signals are given below. Figure 17 shows idealized timing waveforms around IC6. In practice delays are only those of t.t.l. gates and the narrower pulses will not be seen to actually reach 0 V or +5 V.

IC6 pin 3 (10 MHz) - 3 V p-p or greater, an approximate square wave
IC6 pin 11 (10 MHz) - From internal standard, 3 V p-p or greater
IC6 pin 5 (10 MHz) - Negative-going pulses from t.t.l. 'high'
IC6 pin 8 (10 MHz) - Positive-going pulses from t.t.l. 'low'
TR1,TR2 collectors - nominally +12 V

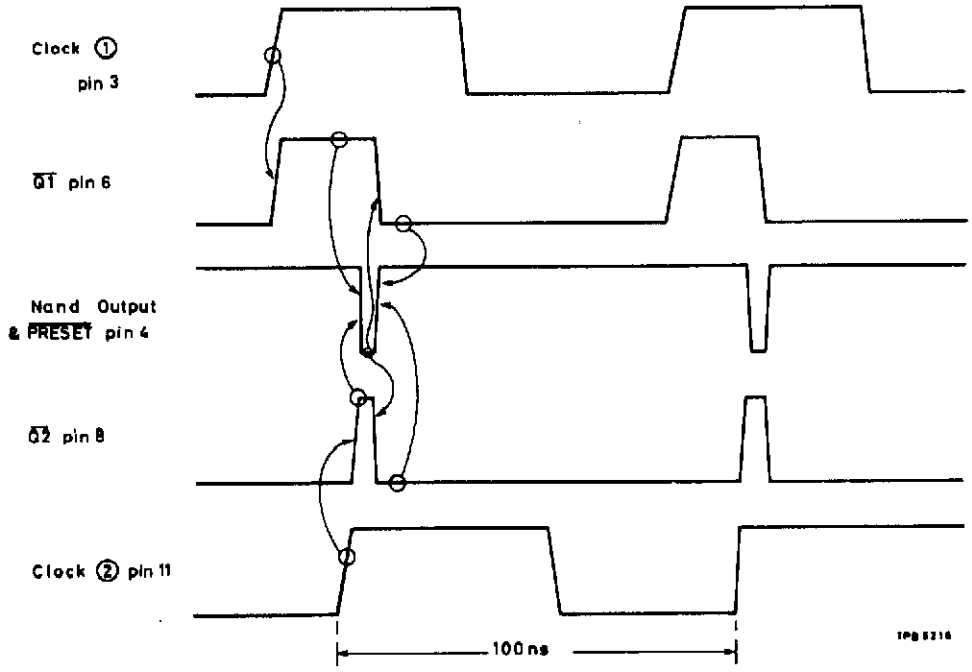


Fig. 17 160 MHz phase detector IC6, timing signals

131. Internal/External frequency standard. Apply an external frequency standard of 1,5 or 10 MHz. Ensure that the internal link from IC8 to IC7 is set for the frequency standard in use. Select 2022 to CARR FREQ, EXT and check the following:-

IC34 pin 3	-	Squarewave, equal to the frequency standard
IC12 pin 1	-	+10 V; indicates that the amplitude of the external standard is sufficient Error No. 11 should show on the display if this voltage is low
IC2 pin 3	-	Inverted version of IC34 pin 3 waveform.

132. Waveforms similar to those shown in Fig. 18 should be seen in the proximity of IC7. The voltage present on TR3, TR4 collectors will depend on the difference between the internal and external frequency standards.

IC12 pins 7,8	-	-10 V
IC12 pin 6	-	+10 V
IC12 pin 10	-	+0.9 V

If an error is detected by the microprocessor, AA2, it will continually select and deselect the external standard. IC2, pin 2, therefore will be continually taken 'high' and 'low' with a repetition time of approximately 250 ms.

133. Internal modulation source; divider and filter. Select AM, INT, MOD ON, from the front panel and check for the following:-

IC14 pin 14	-	TTL 'low'
IC14 pin 12	-	10 kHz square wave
IC14 pin 13	-	1 kHz square wave
IC21 pin 1	-	1 kHz square wave with rounded leading and trailing edges
IC21 pin 7	-	1 kHz sinewave level variable between 0.85 V and 1.6 V p-p varied by R43 setting

134. Synthesizer frequency errors (AA1). If a frequency error has been traced to AA1 board then the information following should enable the fault to be identified. Frequencies selected for testing should be restricted to the fundamental octave of the synthesizer (250 - 500 MHz).

135. Frequency errors less than 40 kHz. Errors in this range are likely to be caused by a fault in the 'Fractional N' system. Check the following:-

IC23 IC24	}	12-bit data latch
IC25 IC26 IC27	}	12-bit adder
IC29 IC30	}	8-bit adder. Sums 8 most significant bits of IC25-27 with 96_{10} (to cause accumulator to overflow at 4000_{10})
IC31 IC32	}	12-bit latch

IC33	Digital-to-analogue converter operating with 8 most significant bits of the accumulator output
TR9/10,	Voltage controlled delay 2-4 ns.

136. Set the CARR FREQ to 250 MHz and using the Δ facility increment the frequency by 10 Hz. Bit D_0 of IC23 will be set and the accumulator formed by IC23-27, IC29-32, will continually count up to 4000_{10} and then reset. The repetition rate will be 10 Hz with one 10 Hz increment applied.

IC33 pin 5	-	-4 V d.c. Varies inversely with carrier frequencies between 250-500 MHz.
IC12 pin 14	-	Staircase waveform comprising 256 steps with a 100 ms period, 4 V p-p amplitude, giving the appearance of a positive-going ramp.
IC32 pin 9		TTL waveform, normally logic 'high', going low to
IC31 pin 9		reset counters etc. very briefly.
TR9 base	-	Narrow negative-going pulses with a 25 µs period.
TR9 collector	-	Narrow positive-going pulses with a 25 µs period. Positive $\frac{dV}{dt}$ approximately 5 V in 100 ns. The loading of an oscilloscope probe will affect this slightly.
TR10 collector	-	Short positive-going pulses with a 25 µs period.

137. Waveforms at key locations within the synthesizer can be seen using IC11b,Q output to synchronize the oscilloscope.

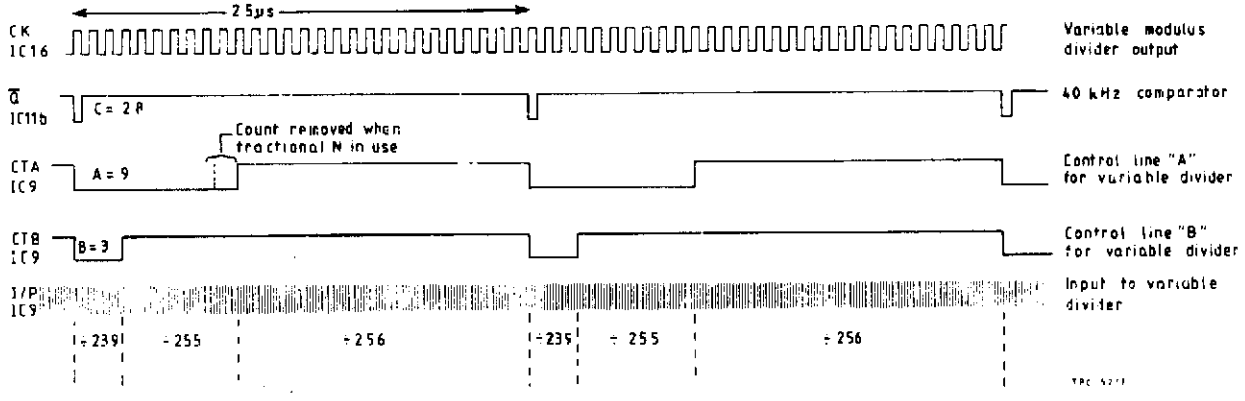


Fig. 18 Synthesizer drive and control waveforms

The following example shows how the synthesized frequency (fractional N component, <40 kHz steps, excluded) is derived

$$Fs = (239x3 + 255x7 + 256x18)x40\ kHz$$
$$= 284.4\ MHz$$

Note ...

The frequency of the clock waveform to IC16 will change as the division ratio changes.

138. Frequency errors between 40 kHz and 10.24 MHz. The most likely cause of faults in this area is the four modulus divider. The following devices should be checked

IC9 IC10c	4 modulus divider and inverter.
IC3 IC19	8-bit data latch. Only the two least significant bits are used from IC19. Binary multiples of 40 kHz.
IC4 IC5	4-bit down counters. These control the length of time IC9 divides by a particular number.
IC10a,b IC11a	Allows modification of division ratio; enables the introduction of the fractional N component.

139. Select CARR FREQ, 327.67999 MHz and using Δ facility, decrement by 10 Hz. IC9 should then be dividing by 256 for most of the time (every 100 ms it will divide by 255). Check also IC10 pin 8 for a square wave with a frequency of 1.28 MHz. Voltage swing should satisfy normal t.t.l. requirements.

140. At frequencies other than multiples of 10.24 MHz (with a negative offset of less than 40 kHz), dividers, IC4 and IC5 will be active. If these malfunction it is possible that the loop will not respond fast enough to give a stable output from IC10. To overcome this introduce each one separately:-

Set CARR FREQ to 327.60 MHz
IC4 pin 12 - 25 µs repetition rate. Mark space ratio 31:1
IC10 pin 6 - 25 µs period. Mark space ratio 30:2

As further 40 kHz decrements are introduced the voltage will remain 'low' for one more $\frac{25}{32}$ µs period in both cases

Set CARR FREQ to 327 MHz
IC5 pin 12 - 25 µs repetition rate. Mark space ratio 31:1

Now as additional frequency decrements of 640 kHz are introduced, the waveform should remain 'low' for additional $\frac{25}{32}$ µs periods.

Note ...

A ripple with a frequency of 1.28 MHz may be seen on the waveforms. Providing the magnitude of this does not affect the t.t.l. 'high' or 'low' levels this is not significant and can be ignored.

141. Frequency errors of 10.24 MHz or greater. Frequency errors caused by AB1 board are considered to have been dismissed as a possibility which then limits the fault to dividers IC16, IC17 and their associated components.

IC13	6-bit data latch. Data is in the form of 10.24 MHz multiples.
IC16 IC17 IC11b	Connected as a presettable counter. Normal range of division ratios is 25 to 49.
IC15b	Combines the fraction N overflow signal with the output of the final divider.

142. Set CARR FREQ, 327.64 MHz. IC16 will route the clock signal through unchanged whilst IC17 will divide by two. Monitor IC16 pins 11 and 12 using pin 11 to synchronize the oscilloscope. A positive-going pulse of approximately 0.78 µs duration should be seen on pin 12. As increments of 10.24 MHz are entered a wider pulse should be seen, this will be delayed by one more clock period each time. Eventually the division ratio of IC17 will increase to three and IC16 pin 12 will go 'high' immediately after the parallel load command on pin 11. There will now be three longer duration pulses on pin 12 in every phase comparator cycle (25 µs).

143. If a frequency counter with a ratiometric function is available it should be connected to IC16 pin 14 (frequency should be in the range 1-2 MHz) and IC11 pin 8 (40 kHz). Second function 3 should be used to change the division ratio by altering the contents of latch 34. Check that the value from the counter coincides with the decimal equivalent of the data in the latch.

Note ...

The oscillators must be switched over in order to cover the full octave of 250-500 MHz.

i.e.	Latch data	Set carrier frequency
	011001 - 100010	317.4 MHz
	100011 - 110000	471 MHz

144. 40 kHz Phase comparator and loop filter. Check the phase comparator IC22 and its associated circuit,

IC22 pin 3	-	40 kHz t.t.l. signal. Mark space ratio 2:3
IC22 pin 11	-	40 kHz t.t.l. signal. Mark space ratio ≈1:50 dependent on the synthesizer frequency
TR7,8 bases	-	+2.5 V
TR7,8 collectors	-	+2.5 V
TR7,8 emitters	-	Very narrow negative and positive-going pulses respectively

Timing waveforms can be seen in Fig. 17.

The voltage on IC28 pin 6 will vary, typically between +2.5 V and +16 V as the carrier frequency is changed from between 250 - 352 MHz and 353-499 MHz.

145. Phase comparator. Carry out the following checks:-

IC14a pin 7	-	40 kHz t.t.l. signal. Mark space ratio 1:4
TR5 emitter	-	+12.7 V
TR6 emitter	-	-9 V
TR5,6 collectors	-	Positive-going ramp -9 V to +12.7 V repetition rate 25 µs. Slew rate 1.2 V/µs

Connect an oscilloscope probe to the junction of R42/IC18 pin 7 and temporarily connect a wire between PLT, pin 10 to a supply of +12 V and -12 V. Check that when +12 V is applied the rising edge of the displayed 40 kHz square wave moves to the right (retards) and has a t.t.l. 'low' level output. Replace the +12 V supply with -12 V and check that the displayed waveform rising edge moves to the left (advances) and that the signal now has a t.t.l. 'high' level output.

146. Frequency synthesizer latch address data. The control data for AA1 is latched on AA2 microprocessor as shown in the table below.

TABLE 19 FREQUENCY SYNTHESIZER LATCH ADDRESS DATA

Address number	Description	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
31 IC23	10 Hz positive frequency increments	10 Hz	20 Hz	40 Hz	80 Hz	160 Hz	320 Hz	X	X
32 IC24	640 Hz positive frequency increments	640 Hz	1.28 kHz	2.56 kHz	5.12 kHz	10.24 kHz	20.48 kHz	X	X
33 IC19	2 bits of 2.56 MHz negative frequency increment. Control of phase modulator and external std.	-2.56 MHz	-5.12 MHz	EXT. STD. ON	LF FM ON	LF FM OFF	1 kHz ON	X	X
34 IC13	10.24 MHz positive frequency increments	10.24 MHz	20.45 MHz	40.96 MHz	81.92 MHz	163.84 MHz	327.68 MHz	X	X
35 IC3	40 kHz negative frequency increments	-40 kHz	-80 kHz	-160 kHz	-320 kHz	-640 kHz	-1.28 MHz	X	X

Microprocessor (AA2)

147. +21 V EAROM supply rail. Check that the following voltages are present.

D2 cathode - +6.2% ±5%
TP2 - +4.5 V
IC1 pin 7 - +1.2 V ±0.5 V
IC1 pin 1 - +8 V
IC1 pin 3 - +4.5 V
TR1 collector - +21 V

148. Parallel to serial converter. If the instrument responds to key presses it is likely that the microprocessor is serviceable. If key presses do not give the correct response monitor the following points in the 'static' condition using an oscilloscope and probe (that is with no keys pressed or GPIB commands occurring).

IC11 pins 1,9,10,11 - Should be t.t.l. 'high' level for most of the time.
IC2 pins 3,6,8,11 - Normally 'high'.
IC13 pins 3,6,11 - Complex data activity
IC14 pins 2,7,10,11 - Normally 'low'

149. Synthesizer drive latches. Check IC15 address latch, first select CARR FREQ 327.6 MHz followed by frequency increments given in the table below; monitor in each case IC15 outputs Q0 to Q4, as indicated using a logic probe.

TABLE 20 SYNTHESIZER FREQUENCY ADDRESS DECODER OUTPUTS

IC15 pin No.	Size of frequency step				
	10 Hz	640 Hz	40 kHz	2.56 MHz	10.4 MHz
2	⊔	X	X	X	X
5	X	⊔	X	X	X
7	X	X	X	⊔	X
10	X	X	X	X	⊔
12	X	X	⊔	X	X

Note ...

⊔ Logic probe will normally be lit then temporarily turned off.

150. Check IC16 data latch; first select CARR FREQ 327.6 MHz followed by a 10 Hz frequency increment. Keeping the UP key ↑ pressed monitor the output lines of IC16 using a logic probe. Check that the sequences listed below can be obtained on pins 2,5,7,10,12 and 15 as shown in the table below.

TABLE 21 DATA LATCH INCREMENT SEQUENCE

IC16 pin No.	Transitory sequence
2	One 'flash' on the logic probe per increment
5	Flashes for two increments, then off for two increments
7	Flashes for four increments, then off for four increments
10	Flashes for eight increments, then off for eight increments
12	Flashes for sixteen increments, then off for sixteen increments
15	Flashes for thirty two increments, then off for thirty two increments

151. Clock divider. Check that the following waveforms are present.

IC17 pin 1 - 2.5 MHz squarewave
IC17 pin 6 - 156.25 kHz squarewave
IC17 pin 8 - 9.765 2/3 kHz squarewave
Other lines only change at approximately 15 minute intervals although IC18 can be checked for basic operation.
IC18 pin 7 - ≈600 Hz squarewave

152. Microprocessor system. Check that a 5 MHz squarewave is present at IC2, pin 1. Also check that IC2, pin 36 logic level is normally 'high' and IC2, pin 7, normally 'low'. Complex waveforms on all the address and data lines may be expected, especially at power on. Suspect any lines that do not change state at all. Similarly, the decoded address lines feeding IC5 - IC10 should toggle at power on (and if it is responding to key presses, then during keyboard interrogation also).

RF processing board (AB1)

153. 160 MHz oscillator. If a 500 Ω oscilloscope probe connected across R6 gives no indication of a 160 MHz waveform (carrier frequency must be set to below 62.5 MHz), then the metal box covering the three voltage controlled oscillators must be dismantled. Care should be taken to ensure that the mating surfaces are kept clean and in particular are kept free of solder splashes on the nickel plated mating areas of the p.c.b.

154. First check that the d.c. conditions on TR1 and D1 are correct then check IC1 and IC2 voltages also.

TR1 drain/R2 junction	-	+8.4 V
TR source	-	+1.6 V
D1 cathode	-	+15.6 V (+12 V with box lid on)
Check C3,C4,C7 serviceability		
IC1 pin 1	-	+0.85 V ±0.1 V
IC1 pin 5	-	+6.5 V ±0.5 V
Similar voltages should be present on IC2		

155. 160 MHz modulator and level control. Check that with a 500 Ω oscilloscope probe connected across R6 the level is approximately -22 dBm. Also check that, with no modulation applied, the voltage at the junction of R10/R11 is a nominal 0 V and TR3 emitter voltage is +0.6 V. Set RF LEVEL, -11 dBm, CARR FREQ, 10 MHz and check the following voltages:-

D3 cathode	-	+0.6 V
Junction of D2/D4 cathodes	-	-0.63 V
'ALC LF' test point	-	typically +6 V
Reset RF LEVEL to -10 dBm (do not use increment facility) 'ALC LF' test point	-	typically +7.1 V

156. BFO mixer. Set CARR FREQ, 10 MHz, RF LEVEL, -11 dBm. Using a 500 Ω oscilloscope probe check at the points shown below that level, frequency and distortion are in agreement with the figures given.

Across R71 Freq. 170 MHz, Level -16 dBm, Distortion <20 dBc second harmonic
L4 to ground Freq. 160 MHz, Level -35 dBm, Distortion <35 dBc second harmonic
(Pin 1 of X1)
Across R83 Freq. 10 MHz, Level -40 dBm.

157. BFO output amplifier and levelling loop. Set CARR FREQ, 10 MHz, RF LEVEL -11 dBm and check the following:-

TR11 base	-	+11.5 V
TR11 collector	-	+6 V
TR12 base	-	+0.7 V
TR12 collector	-	+5 V
D33 anode	-	-0.33 V
D44 cathode	-	+0.33 V
IC12 pin 7	-	+6 V

158. 250-500 MHz oscillators. Set CARR FREQ, 250 MHz followed by a frequency of 353 MHz. The following voltages should be noted:-

	250 MHz	352 MHz
R24	0 V	+5 V
TR5 collector	-12 V	-11.35 V
TR6 collector	-0.55 V	-12 V
TR8 collector	-11.35 V	-12 V
TR9 collector	-12 V	-0.55 V
Voltage drop across R29	-	1.9 V
Voltage drop across R39	1.9 V	-
PLAD, pin 16	+2 V	+2 V

Monitor the signal level across R48 with a 500 Ω probe and check that this is approximately -25 dBm. If one or other of the oscillators fails to operate correctly it will be necessary to remove the metal screen covering the oscillators. As mentioned previously, care must be taken to ensure that all mating surfaces are kept clean to maintain screening efficiency. As before select the two carrier frequencies 250 MHz and 353 MHz and check for the following voltages:-

Carrier frequency	250 MHz	353 MHz
TR7 collector	+12 V	+8.25 V
TR10 collector	+8.25 V	+12 V

159. Check for leakage in D5,D6,D7 and the correct operation of each diode junction. Decoupling and phase correction capacitors should also be checked. If functioning correctly each oscillator should oscillate strongly even if capacitive loads (i.e. fingers) are introduced.

Note ...

> TR10 is intentionally fitted with markings facing the p.c.b., replacement items should also be fitted in the same position.

Finally check that the four buffer amplifiers IC7-IC10 have the following voltages present:-

IC7-IC10 pin 1 - +0.85 V ±0.1 V
pin 5 - +6.5 V ±0.5 V

160. Signal divider (two stage IC11a,b). Set CARR FREQ, 62.5 MHz both dividers IC11a and b will now be in operation. Check that the following voltages are present;-

IC11 pin 11 - +3.6 V
IC11 pin 10 - +3.6 V
IC11 pin 7 - +3.6 V
Point (F) - +0.2 V (Points (A) to (F) are shown in Chap. 7 Fig. 8)
Point (A) - +0.2 V
D15/18 junction - +5.7 V
Point (B) - +7.8 V

A signal of approximately -12 dBm should be seen across R69 using a 500 Ω oscilloscope probe, check also for the following:-

D16 anode - +0.95 V
D11 anode - +1.7 V

Note ...

Switching diode bias is drawn through the two low-pass filters LPF "STOP 375 MHz" and LPF "STOP 187.5 MHz". Attempts therefore to measure signal levels should be made with a capacitively coupled probe. Excessive harmonic distortion at the outputs of the divider stage (>-25 dBc of second harmonic across R69, and from the junction C91/R16 and ground) or a raised noise floor indicate a potentially defective divider; particularly if the drive levels have been checked and found to be satisfactory.

161. 250-500 MHz switch. Set CARR FREQ, 250 MHz, this selection will effectively switch off IC11a,b, dividers and cause diode network D8,D9, D10 to re-route the r.f. signal through to the "STOP 750 MHz" low-pass filter. Check the following:-

Point (E) - +0.1 V
D10 cathode - +2.5 V
D9 anode - +1.6 V

162. Mixer driver/doubler drive and levelling loop. Set CARR FREQ 500 MHz, check using a 500 Ω oscilloscope probe the signal level across R64. This should be approximately -15 dBm. Also check the following voltages:-

R63/C122 junction - +5 V
D21 anode - +3.9 V
ALC doubler voltage - +3.7 V
D22 cathode - +3 V
D24 anode - +3.5 V
IC13 pin 1 - +3.1 V
IC13 pin 8 - +12 V

Note ...

D24 detects the negative peaks of the drive waveform present at IC13 output. Thus the d.c. level on the anode will decrease as the r.f. voltage increases. Attach a capacitively coupled 500 Ω probe between the junction of R80/D26 and ground. The power level at this point should be approximately -10 dBm with a second harmonic distortion better than -20 dBc.

163. Signal doubler and band-pass filter. Set CARR FREQ, 500 MHz, and check the following voltages:-

D26 cathode - +4.1 V
R90/C103 junction - -0.2 V } Will depend on
D27/D28 or D29/D30 junctions - -0.03 V } r.f. signal level.
IC3 pin 1 - +0.85 V ±0.1 V
IC3 pin 5 - +6.5 V ±0.5 V

164. The band-pass filter comprising D34,D35 and T6 cannot be adjusted. However a check can be made on the filter tracking. Monitor the voltage and the junction of R27,R107 whilst incrementing the carrier frequency in 100 MHz steps starting from 500 MHz. Compare the results with the values in Table 22.

TABLE 22 TYPICAL BAND-PASS FILTER TRACKING VOLTAGES/CALIBRATION DATA

Carrier freq.	Filter tuning voltage	EAROM data
500 MHz	5.5 V	60
600 MHz	9.0 V	100
700 MHz	11.5 V	120
800 MHz	14.0 V	150
900 MHz	18.0 V	190
1000 MHz	23.5 V	250

165. Check the voltage drop across R97 and R107, this should be negligible, also check

Point (D) - +0.25 V
D32 anode - +1 V

166. 62.5-1000 MHz output amplifier and levelling loop. Set CARR FREQ, 1000 MHz, RF LEVEL, -11 dBm. Check the following voltages:-

D38 cathode - +0.06 V
D41 cathode - +0.06 V
TR13 emitter - +11.6 V
IC14 pin 1 - +3.1 V
IC14 pin 8 - +12 V
Signal level across R93 - -16 dBm
(using capacitively coupled 500 Ω probe)
D43 cathode - +0.25 V
Check that D50 is reverse biased
IC15 pins 2,3 - +0.1 V
IC15 pin 6 - +10 V

167. Couple a 50 Ω external load to the RF OUTPUT socket of the instrument and select the r.f. levels shown in Table 23. Monitor in each case the test points indicated.

TABLE 23 62.5-1000 MHz OUTPUT AMPLIFIER DRIVE CONDITIONS

RF level	PLAD pin 3	D43 cathode	IC15 pin 6	TR13 emitter
-10 dBm	+0.14 V	-0.11 V	+10.1 V	+11.7 V
-6 dBm	+0.26 V	0 V	+10.1 V	+11.7 V
0 dBm	+0.58 V	+0.31 V	+10 V	+11.6 V
+6 dBm	+1.22 V	+0.96 V	+9.6 V	+11.5 V

168. Control logic states. IC4, IC5 and IC6 are used to control the switching of diodes and dividers as the frequency bands change. Table 24 gives the different states used and their associated logic levels.

TABLE 24 FREQUENCY BAND SWITCHING, LOGIC LEVELS

Frequency band	PLAD pin 6 A_0	PLAD pin 11 A_1	PLAD pin 7 A_2	"OSC HIGH"	A	B	C	D	E	F	G
10 kHz-16.5 MHz	0	1	1	0	1	0	1	1	1	0	1
16.5-62.5 MHz	0	1	1	1	1	0	1	1	1	0	1
62.5-88.25 MHz	0	0	0	0	0	1	0	1	1	0	0
88.25-125 MHz	0	0	0	1	0	1	0	1	1	0	0
125-176.5 MHz	1	0	0	0	1	0	0	1	1	0	0
176.5-250 MHz	1	0	0	1	1	0	0	1	1	0	0
250-353 MHz	1	1	0	0	1	1	0	1	0	1	0
353-500 MHz	1	1	0	1	1	1	0	1	0	1	0
500-706 MHz	0	1	0	0	1	1	1	0	0	1	0
706-1000 MHz	0	1	0	1	1	1	1	0	0	1	0

INSTRUMENT CALIBRATION

169. This section contains information for the overall realignment of the instrument with details of preset components, affected circuits and the use of second function controls where these are needed in recalibration procedures.

170. After completing repairs to a circuit or replacement of a board it may be necessary to carry out realignment. If a full overall realignment is required it should be carried out in the order shown in Table 25 below.

TABLE 25 RECALIBRATION ORDER

Order	Adjustment	Table of reference	2ND FUNCT
1	Set +12 V	27	None
2	+5 V	27	None
3	-12 V	27	None
4	+24 V	27	None
5	+21 V	29	None
6	LCD off	26	None
7	1 kHz level	28	None
8	250 MHz	30	None
9	353 MHz	30	None
10	160 MHz	30	None
11	160 MHz "LF AM Mod".	30	None
12	Correct jitter	27	None
13	Cal. band-pass tracking	27	193
-	and Notch	30	3
14	Cal. RF power >62.5 MHz	27	192
15	Cal. RF power <62.5 MHz	27	192
16	Cal. AM >62.5 MHz	27	194
17	Cal. AM <62.5 MHz	27	194

continued ...

TABLE 25 RECALIBRATION ORDER (continued)

Order	Adjustment	Table of reference	2ND FUNCT
18	External mod.	27	None
19	Set LF FM and	27	191
-	FM tracking	15	191
20	Set ϕM	27	None
21	Set Int. Std. Freq.	27	None

171. If only one board is affected and a full overall realignment procedure is not needed then the individual board can be realigned with reference to one of a number of Board Realignment tables that follow. Some of the tables make reference to certain alignment procedures using second functions 191-194. A comprehensive description of these is also included in the following paragraphs to assist users unfamiliar with their operation.

Note ...

Before any adjustments are made all screening covers should, where possible, be firmly fitted.

Second function ´191´ FM tracking calibration

172. The f.m. tracking calibration data comprises two tables of calibration points. These are listed in Table 15. To enter data, carry out the following procedure:-

(1) Unlock the instrument to allow second level operation.

(2) Select CARR FREQ, 250 MHz and a carrier frequency increment, of 4.12 MHz, FM INT, 99.9 kHz.

(3) Enter 2ND FUNCT 191.

(4) Monitor the actual deviation obtained on a modulation meter (2305). If no data has been stored, enter the value shown in Table 15 Typical FM tracking data e.g. 194. Now using the up (↑) or down (↓) key adjust the calibration data until the modulation meter reads closest to the value 99.9 kHz and press the STORE key, (see following Notes before calibrating).

(5) Reselect CARR FREQ followed by the up key to increment the carrier frequency by 4.12 MHz. Re-enter 2ND FUNCT 191 and the approximate data, (e.g. 204) then adjust the value using the up or down key as described in step (4) and STORE. Repeat the above procedure for succeeding 4.12 MHz increments entering data in each until reaching a carrier frequency of 353 MHz. At this point re-select CARR FREQ 352.999 MHz, 2ND FUNCT 191, enter data and STORE.

(6) Select CARR FREQ, 353 MHz and a carrier frequency increment of 5.88 MHz, re-enter 2ND FUNCT 191 then continue entering data as previously described in steps (4) & (5) until reaching a carrier frequency of

500 MHz. At this point select instead CARR FREQ 499.9999 MHz, re-enter 2ND FUNCT 191, enter data and STORE. This completes the FM tracking.

Notes ...

(1) The audio frequency response must have previously been adjusted using A2, R58, 'SET LF FM'.

(2) A suitable bandwidth must be selected on the modulation meter to avoid errors due to demodulated noise e.g. (50 Hz - 15 kHz).

Second function '192' RF level calibration

173. The r.f. level is calibrated at 11 selected reference points, each point is numbered from 00 to 10 with the selected point displayed in the modulation window. Calibration is carried out first at 15 MHz and then in 100 MHz steps from 100 to 1000 MHz.

(1) Unlock the instrument to allow second level operation.

(2) Select CARR FREQ, 15 MHz, RF LEVEL, 0 dBm and an r.f. level increment of 10 dB.

(3) Enter 2ND FUNCT 192.

(4) Monitor the RF OUTPUT using a Power Meter (6960) and Power Sensor (6912).

(5) Enter a value of data that will give a reading of 0 dBm on the power meter using the up or down keys as required (there is no auto incrementing on this function).

(6) Select RF LEVEL then the down key to obtain a level of -10 dBm; adjust AB1, R101, 'LF ALC LOW' for a 10 dB difference between this reading and that obtained in step (5). (dB rel. key can be used on 6960). Reselect the up key to obtain 0 dBm output and iterate until the values obtained in step (5) and (6) are as close to 0 dBm and -10 dBm as possible, then STORE the calibration data.

(7) Select CARR FREQ, 200 MHz and a carrier frequency increment of 100 MHz, RF LEVEL, 0 dBm. Now repeat the procedure described in steps (4) and (5) decrementing the level to -10 dBm and in this case adjusting A2, R84, 'HF ALC LOW' to obtain the 10 dB difference.

(8) Select CARR FREQ and using the down key decrement the carrier frequency to 100 MHz, select RF LEVEL, 0 dBm. Re-enter 2ND FUNCT 192 followed by a value of data to obtain a reading of 0 dBm on the power meter then STORE. Now select CARR FREQ and with the up key increment the carrier to select a frequency of 300 MHz. Re-enter 2ND FUNCT 192 and enter data to give a power meter reading of 0 dBm and STORE. Continue to increment the carrier frequency in 100 MHz steps entering data and storing in each case until reaching the last data point, 10 (1000 MHz). This completes the RF level calibration.

Second function ´193´ voltage tuned filters (VTF) calibration

174. The VTF or Output harmonic control calibration table consists of 6 points calibrated in 100 MHz steps from 500 MHz to 1000 MHz. Each point is numbered from 00 to 05 with the selected data point displayed in the modulation window. Calibration is carried out as follows:-

(1) Unlock the instrument to allow second level operation.

(2) Select CARR FREQ, 500 MHz and a carrier frequency increment of 100 MHz.

(3) Monitor AB1, ´ALC HF´ test point with a digital voltmeter.

(4) Enter 2ND FUNCT 193.

(5) Enter or adjust data to obtain the greatest positive reading possible (typically +10 V), then press the STORE key to terminate the entry. Typical values of calibration data expected can be seen in Table 16. Values of voltage shown in that table however cannot be compared because they are taken from a different circuit reference.

(6) Select CARR FREQ followed by the up key to select a carrier frequency of 600 MHz. Repeat the procedure described from step (4) and continue the calibration for each step until reaching the last data point 05, (1000 MHz). This completes the VTF calibration.

Second function ´194´ AM calibration

175. Only two points are calibrated. At point 00 data is entered at a carrier frequency of 15 MHz and point 01 at a carrier frequency of 100 MHz. 00 or 01 is displayed in the modulation window after selecting 2ND FUNCT 194 and the relevant carrier frequency. Calibrate as follows:-

(1) Unlock the instrument to allow second level operation.

(2) Select CARR FREQ, 15 MHz, AM, INT, 95%, RF LEVEL, 0 dBm.

(3) Monitor the RF OUTPUT socket using a Modulation Meter (2305).

(4) Enter 2ND FUNCT 194.

(5) Enter or adjust data to obtain a mod. meter reading of 95% then STORE to terminate the entry.

(6) Select CARR FREQ, 200 MHz, AM, INT, 90% and an r.f. level increment of 10 dB.

(7) Again enter 2ND FUNCT 194 and enter or adjust data to obtain a reading on the mod. meter of 90% then STORE the value.

(8) Select RF LEVEL followed by the down key to give a power level reading of -10 dBm. Adjust A2, R90, ´CORRECT DETECTOR´ to give a mod. meter reading of 90% a.m. Reselect up and down keys and repeat the adjustment until a reading of 90% is obtained at both 0 dBm and -10 dBm. This completes the AM calibration.

Second function '195' calculation and storage of amended EAROM checksum

176. If the instrument has been recalibrated, or if data in the EAROM, AA2, IC10 has been accidentally erased, or if an unserviceable EAROM has been replaced then a new checksum should be stored and initialization should be carried out. When recalibrating the instrument following EAROM replacement it should not be necessary to adjust any of the internal preset components; i.e. calibration data can be found by accessing the data from the front panel second function controls and in the following order 191,193,192,194. Enter the calibration information for each of the above second functions and store in each case. When this is completed select 2ND FUNCT 195 and STORE. The instrument will re-calculate the checksum, store this in the non-volatile memory and display 000 to indicate completion.

EAROM initialization

177. Data stored within the EAROM but not part of the checksum will also have to be re-entered. A replacement EAROM is normally supplied with all '1's stored, therefore flags on most second functions and other settings referred to have been arranged such that the most useful are selected when a replacement EAROM is installed. Each of the following should be checked, re-entered if necessary, depending on individual user requirements, and in the order given below.

(1) RF level offsets data (second function 15) off '0' on '1'. This facility must not be used until the instrument is calibrated.

(2) Checksum data for calibration values (second function 195).

(3) Timer information, both for the resettable (second function 9) and the fixed timer (second function 199) see Note below.

(4) Identity strings (second function 190) Chap. 4 para. 192 refers, these can be recalled using either second functions 5 or 11.

(5) User defined strings entered by means of second function 12.

(6) Instrument settings stored by the user. Store protection (second function 196) and Display blanking of recalled stores (second function 197). Each store has a separate checksum which is automatically entered on storing a valid setting. Stores not having a value entered will initiate a EAROM recall error message 15 when recalled.

(7) Calibration information from second functions 191-194.

(8) External frequency standard10,5 or 1 MHz (second function 10).

(9) If the optional GPIB facility is fitted set the address as required (second function 2).

Note ...

The total instrument operating time indicator, if accessed by second function 198 will probably read 131, 071 hours. After approximately 15 minutes instrument running time this will overflow and reset to 0 hours.

TABLE 26 A1 KEYBOARD AND DISPLAY BOARD ALIGNMENT

Adjustment	Test equipment	Method	Adjustment window/Comments
R2 "LCD off"	Visual examination only required.	Adjust R2 whilst observing the segment of the display from an acute angle. Adjust so that "off" segments are barely turned off.	Some contrast may be lost if incorrectly adjusted.

TABLE 27 A2 POWER SUPPLY AND CONTROL BOARD ALIGNMENT

Adjustment	Test equipment	Method	Adjustment window/Comments
R5 "Set +12 V"	d.v.m.	Detach all board external loads and adjust to +12.1 V.	±0.1 V
R15 "Set +5 V"	d.v.m.	Detach all board external loads and adjust to +5.05 V	±0.05 V
R8 "Set -12 V"	d.v.m.	Detach all board external loads and adjust to -12.1 V.	±0.1 V
R89 "Set +24 V"	d.v.m.	Detach all board external loads and adjust to +24.25 V.	±0.25 V
R67 "Correct Jitter"	Modulation meter and head phones.	Select CARR FREQ, 250.0005 MHz. Listen for a tone and null this.	If this is incorrectly set there may be additional coherent signals present with the carrier frequency.

continued ...

TABLE 27 A2 POWER SUPPLY AND CONTROL BOARD ALIGNMENT (continued)

Adjustment	Test equipment	Method	Adjustment window/Comments
´Cal. band-pass filter´	d.v.m.	Select CARR FREQ, 500 MHz Monitor ´ALC HF´ test point on AB1. Adjust CAL DATA (using 2ND FUNCT 193) for greatest positive reading. Repeat at 100 MHz intervals up to 1 GHz.	Increments are extremely fine and a setting within ±5 counts will give adequate results.
´Cal. RF power and R84 HF ALC low´	RF power meter	Select CARR FREQ, 200 MHz, RF LEVEL 0 dBm. Adjust for 0 dBm output (using 2ND FUNCT 192). Select RF LEVEL -10 dBm and adjust R84 then optimize with 0 dBm adjustment. Finally calibrate at 100 MHz and subsequent 100 MHz intervals up to 1 GHz.	Adjust R84 to give a 10 dB difference between the 0 and -10 dBm readings at 200 MHz.
´Cal. AM >62.5 MHz´ and R90 ´Correct det´.	Modulation meter	Select CARR FREQ, 200 MHz, RF LEVEL, 0 dBm, AM, 80%. Adjust (using 2ND FUNCT 194) until reading is correct. Select RF LEVEL, -10 dBm, AM, 90% and adjust R90 for correct AM depth. Re-check cal. data setting at 0 dBm.	
´Cal. RF power´ and R101 (AB1) ´LF ALC low´	Power meter	Select CARR FREQ, 15 MHz, RF LEVEL, 0 dBm. Adjust (using 2ND FUNCT 192) cal. data.	It is unlikely that there will be a significant difference in the calibration data.

continued ...

TABLE 27 A2 POWER SUPPLY AND CONTROL BOARD ALIGNMENT (continued)

Adjustment	Test equipment	Method	Adjustment window/Comments
"Cal. RF power" and R101 (AB1) "LF ALC low" (continued)	Power meter	for 0 dBm output. Select RF LEVEL, -10 dBm and adjust R101 (AB1) for -10 dB w.r.t. 0 dBm reading. Recheck the 0 dBm setting.	
"Cal. AM <62.5 MHz".	Modulation meter.	Select CARR FREQ, 15 MHz, RF LEVEL, 0 dBm, AM, 95%. Adjust (using 2ND FUNCT 194) for correct value.	It is unlikely that a significant change in cal. data will be required.
R113 "External Mod"	Modulation meter. Accurate 1 V r.m.s. 1 kHz external source.	Select CARR FREQ, 250 MHz, FM dev., 99.9 kHz. Apply Ext. Mod. source, MOD ALC on. Note the reading. Switch MOD ALC off and adjust R113 for identical dev. reading. Recheck MOD ALC on reading.	
"Cal. FM and R58 Set LF FM"	Modulation meter and Audio source 100 Hz, 10 kHz, 1 V r.m.s.	Select CARR FREQ, 250 MHz, FM dev. 99.9 kHz. Apply 10 kHz Ext. Mod. source, MOD ALC on. Adjust cal. data (using 2ND FUNCT 191) for 99.9 kHz dev. Now set Ext. Mod. source to 100 Hz and adjust R58 for 99.9 kHz dev. Remove Ext. Mod. source and select Int. Mod. and recalibrate at frequencies shown in Table 15.	If calibration number does not change by more than one or two digits, check to see if FM is within specification before proceeding with recalibration.

continued ...

TABLE 27 A2 POWER SUPPLY AND CONTROL BOARD ALIGNMENT (continued)

Adjustment	Test equipment	Method	Adjustment window/Comments
R56 "Set ΦM"	Modulation meter	Select CARR FREQ, 250 MHz, ΦM 9.99 rads. dev. Adjust R56 for the same reading.	Can be demodulated as f.m. and dev. set to 9.99 kHz. 1 kHz internal source frequency is extremely accurate.
(A0)R1 "Int. Std. Adjust".	Frequency counter	Adjust A0R1 for correct reading.	2022 frequency accuracy is directly dependent on this setting.

TABLE 28 AA1 SYNTHESIZER BOARD ALIGNMENT

Adjustment	Test equipment	Method	Adjustment window/Comments
R43 "Set 1 kHz level"	AC voltmeter	Select INT MOD and monitor the voltage on the MOD IN/OUT socket. Adjust R43 for 1.00 V r.m.s.	
(A0)R1 "Int. Std. Adjust".	Adjustment carried out in conjunction with A2 board alignment see Table 27.		
(A2)R67 "Correct jitter"	Adjustment carried out in conjunction with A2 board alignment see Table 27.		Allows for variations in component value.
(A2)R58 "Set LF FM"	Adjustment carried out in conjunction with A2 board alignment see Table 27.		Allows for variations in component value.

TABLE 29 AA2 MICROPROCESSOR BOARD ALIGNMENT

Adjustment	Test equipment	Method	Adjustment window/Comments
R1 "Set +21 V"	Digital voltmeter	⚠ Remove IC10 if fitted. Monitor TP3 and adjust R1 for +21.0 V. When extracting IC10 use an Insertion/ Extraction tool to protect the integrated circuit and the p.c.b.	±0.1 V. Fit EAROM from previous board if this is serviceable to save further recalibration.
EAROM Recalibration	All recalibration data relating to second functions 191,192,193 and 194.		Should not be necessary to re-adjust preset controls if this is the only requirement.

TABLE 30 AB1 RF PROCESSING BOARD ALIGNMENT

Adjustment	Test equipment	Method	Adjustment window/Comments
C38 "250 MHz"	Digital voltmeter	Select CARR FREQ, 250 MHz. Adjust C38 for 2.0 V on PLAD pin 16.	±0.1 V
C31 "353 MHz"	Digital voltmeter	Select CARR FREQ, 353 MHz. Adjust C38 for 2.0 V on PLAD pin 16.	±0.1 V
C7 "160 MHz"	Digital voltmeter	Select CARR FREQ, 10 MHz. Adjust C7 for 12.0 V on PLAD pin 1.	±1 V

continued ...

TABLE 30 AB1 RF PROCESSING BOARD ALIGNMENT (continued)

Adjustment	Test equipment	Method	Adjustment window/Comments
C18 "LF AM MOD"	Digital voltmeter	Select CARR FREQ, 10 MHz RF LEVEL, 0 dBm. Connect d.v.m. to ALC LF test point and adjust C18 for maximum positive voltage.	Nominally +6 V to +7 V.
"Cal FM and (A2)R58 Set LF FM"	See A2 board alignment (Table 27)		
"Cal RF power and (A2)R84 HF ALC low"	See A2 board alignment (Table 27)		
"Cal RF power and R101 LF ALC low"	See A2 board alignment (Table 27)		
"Cal band-pass filter and L13 Notch"	Digital voltmeter and 500 MHz Spectrum Analyzer.	Calibrate band-pass filter (see A2 board alignment). Note calibration value at 500 MHz. Select CARR FREQ, 499 MHz, RF LEVEL, +6 dBm, (using 2ND FUNCT 3 address 12) enter value noted above into the filter tracking DAC. Adjust L13 for minimum output at 499 MHz.	There will be some effect due to hand capacitance although the adjustment is not critical. Should obtain typically 20 dB rejection from the notch.

continued ...

TABLE 30 AB1 RF PROCESSING BOARD ALIGNMENT (continued)

Adjustment	Test equipment	Method	Adjustment window/Comments
C16 "LF AM mod."	Digital voltmeter	Select CARR FREQ 15 MHz. Monitor "ALC LF" test point and adjust for maximum reading.	The voltage measured will depend on the RF LEVEL selected.
"Cal. AM >62.5 MHz and (A2)R90 Correct det"	See A2 board alignment (Table 27)		
"Cal AM <62.5 MHz"	See A2 board alignment (Table 27)		

TABLE 31 ATTENUATOR ASSEMBLY

Adjustment	Test equipment	Method	Adjustment window/Comments
"CAL RF power"	Power meter	Select CARR FREQ, 15 MHz, 100,200, 300,400,500,600, 700,800,900 and 1000 MHz, RF LEVEL, 0 dBm. Adjust cal. data (using 2ND FUNCT 192) to give 0 dBm output.	No attempt should be made to adjust the frequency compensation screws on the attenuator assembly. Refer to factory.

External frequency standard adjustment (1,5 or 10 MHz)

178. One of three external standard frequencies may be used providing a link on AA1 board is correctly positioned. Access and layout paragraphs give details of accessing AA1 board and Fig. 19 below shows the position of the three link positions for 1, 5 or 10 MHz. Withdraw the link manually from the board (normally selected to 10 MHz) and reposition as required. On completion apply power and using 2ND FUNCT 10 record the current selection and STORE. Further check by selecting 2ND FUNCT 1 "Status" mode that the correct reading is evident in the modulation window.

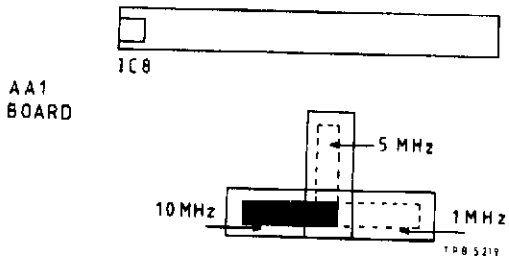


Fig. 19 External frequency standard adjustment (1, 5 or 10 MHz)

Chapter 6

REPLACEABLE PARTS

CONTENTS

INTRODUCTION

1. Each sub-assembly or printed circuit board in this equipment has been allocated a reference designator code, e.g. A0, A1, A2 etc.

2. The complete component reference includes its reference designator as a prefix e.g. A2C1 (capacitor C1 on sub-assembly A2) but for convenience in the text and diagrams the prefix is omitted unless it is needed to avoid confusion. However when ordering replacements or in correspondence the complete component reference must be quoted.

ABBREVIATIONS

3. Electrical components are listed in alpha-numerical order of their complete circuit reference and the following standard abbreviations are used in the 'Description' column :

ADC	analogue-digital converter
CAP	capacitor
CARR	carrier
CARB	carbon
CC	carbon composition
CDE CNV	code converter

CERM	cermet
CF	carbon film
COAX	coaxial
CON	connector
CTR	counter
DAC	digital-analogue converter
DEC/DMX	decoder/demultiplexer
DECOD	decoder
DIL	dual in-line
DIV	divider
DRIV	driver
ELEC	electrolytic
ENCOD	encoder
FEM	female
FF	flip-flop (bistable)
FILTERCON	filtering capacitor
GER	germanium
GP	general purpose
ICA	integrated circuit, analogue
ICD	integrated circuit, digital
IND	inductor
INV	inverter
LD/T	lead through
MF	metal film
MG	metal glaze
MISC	miscellaneous
MO	metal oxide
MP	microprocessor
MP SUPP	microprocessor support
MUX	multiplexer
NET	network
PC	polycarbonate
PETP	(polyester)polyethelene terephthalate
PS	polystyrene
PLL	phase-locked loop
Q/ACT	quick acting
RECT	rectifier
RES	resistor
RV	resistor, variable
RX	receiver
SAPPH	sapphire
SEC	secondary
SH REG	shift register
SIL	silicon
SW	switch

T/LAG	time lag
TANT	tantalum
TOG	toggle
TRANS	transistor
TX	transmitter
VAR	variable
VREG	voltage regulator
W	watts at 70^0C
WW	wirewound
X	miscellaneous item
XL	crystal
!	static sensitive component
% +	asymmetric tolerance

COMPONENT VALUES

4. One or more of the components fitted in the equipment may differ from those listed in this chapter for any of the following reasons:

(a) Components indicated by a * have their values selected during test to achieve particular performance limits.

(b) Owing to supply difficulties, components of different value or type may be substituted provided the overall performance of the equipment is maintained.

(c) As part of a policy of continuous development, components may be changed in value or type to obtain detail improvements in performance.

5. When there is a difference between the component fitted and the one listed, always use as a replacement the same type and value as found in the equipment.

ORDERING

6. When ordering replacements, address the order to our Service Division (address on rear cover) or nearest agent and specify the following for each component required:-

(1) Type# and serial number of equipment.

(2) Complete circuit reference.

(3) Description.

(4) Part number.

#As given on the serial number label at the rear of the equipment; if this is superseded by a model number label, quote the model number instead of the type number.

Circuit Ref	Description	Part Number
ELECTRICAL COMPONENTS		
Unit A0	- SIGNAL GENERATOR	
7. When ordering, prefix circuit reference with A0		
	Complete unit	52022-900C
FS1 FS2	FUSE T/LAG 0.25A 20X5 FUSE T/LAG 0.25A 20X5 } 210V-240V SLOW	23411-045F
FS1 FS2	FUSE T/LAG 0.5A 20X5 FUSE T/LAG 0.5A 20X5 } 105V-120V SLOW	23411-046G
	FUSE HOLDER	23416-192R
IC1	ICA VREG+ LM317T PROG 1A5	28461-726A
PLC	CON PWR MALE 3 FXD	23423-159P
PLP	CON PCB HDR 20 FXD	23435-957C
PLR	CABLE ASSY (PLR-SKS)	43130-091N
PLV	CABLE ASSY (PLV-SKU)	43130-021Y
PLW	CABLE ASSY	43130-030V
PLX	CON RF SMB MALE 50 PCB STR	23444-334Y
PLY	CABLE ASSY (PLY-SKX)	43130-022N
PLZ	CABLE ASSY	43130-031S
PLAE	CABLE ASSY	43130-032W
PLAE	CABLE ASSY (PLAF-SKB)	43130-011B
R1	RV CERM 10K LIN .5W 10%	25748-518H
SA	SW TOG 2CO LEVER MAINS	23462-249Z
SB	SW SLIDE 2CO PANEL MTG	23467-161W
SC	SW SLIDE 2CO PANEL MTG	23467-161W
SKA	CON RF BNC FEM 50 BKHD	23443-442B
SKB	CABLE ASSY (SKB-PLAF)	43130-491A
SKD	CABLE ASSY (SKD-SKR)	43130-012K
SKE	CON 57 FEM 24 FXD PCB EDG GPIB	23435-133X
SKH	CABLE ASSY	43130-014Z
SKJ	CABLE ASSY	43130-010R
SKK	CABLE ASSY	43130-026G
SKL	CABLE ASSY	43130-018Y
SKM	CABLE ASSY	43130-028S
SKN	CABLE ASSY	43130-015H
SKP	CABLE ASSY	43130-027V
SKR	CABLE ASSY (SKR-SKD)	43130-012K
SKS	CABLE ASSY (SKS-PLR)	43130-019N
SKT	CABLE ASSY	43130-020U
SKU	CABLE ASSY (SKU-PLV)	43130-021Y
SKV SKW	CABLE ASSY CABLE ASSY } (SKV-SKW)	43130-016E
SKX	CABLE ASSY (SKX-PLY)	43130-022N

Circuit Ref	Description		Part Number
Unit A0	- SIGNAL GENERATOR	(Contd.)	
SKY	CABLE ASSY } (SKY-SKZ)		43130-017U
SKZ	CABLE ASSY		
SKAA	CABLE ASSY		43130-023L
SKAB	CABLE ASSY		43130-024J
SKAC	CABLE ASSY		43130-025F
SKAD	CABLE ASSY		43130-029W
SKAE	CON RF SMA FEM 50 BKD LG S/BK		23444-513F
SKAF	CON RF SMA FEM 50 FLG S/BK		23444-509J
SKAG	CON PART MIN HOUSING 1 ROW 3P		23435-171R
TR1	TR NSI BD543 40V LOW VCE		28454-750B
T1	TRANSFORMER MAINS TOROIDAL		43490-086G
X1	FAN AX 5V DC 48MM		23535-127B
Unit A1	- KEYBOARD PCB		
8. When ordering, prefix circuit reference with A1			
	Complete unit		44828-781B
C1	CAP CER 1N0 63V 10% PLATE		26383-585M
C2	CAP CER 1N0 63V 10% PLATE		26383-585M
C3	CAP ELEC 100U 6.3V 20% SUBMIN		26421-118L
D1	LAMP LED HLMP1401 2.4V YEL		28624-137D
D2	LAMP LED HLMP1401 2.4V YEL		28624-137D
D3	LAMP LED HLMP1401 2.4V YEL		28624-137D
D4	LAMP LED HLMP1401 2.4V YEL		28624-137D
D5	LAMP LED HLMP1401 2.4V YEL		28624-137D
D6	LAMP LED HLMP1401 2.4V YEL		28624-137D
D7	LAMP LED HLMP1401 2.4V YEL		28624-137D
D8	LAMP LED HLMP1401 2.4V YEL		28624-137D
D9	DI SIL 1N4148 75V JUNC		28336-676J
D10	DI SIL 1N4148 75V JUNC		28336-676J
D11	DI SIL 1N4148 75V JUNC		28336-676J
D12	DI SIL 1N4148 75V JUNC		28336-676J
D13	DI SIL 1N4148 75V JUNC		28336-676J
D14	DI SIL 1N4148 75V JUNC		28336-676J
IC1	ICD DRIV 7225G 32 SEGMENT LCD	!	28467-023H
IC2	ICD DRIV 7225G 32 SEGMENT LCD	!	28467-023H
IC3	ICD FF D 40174 HEX	!	28462-616Y
IC4	ICD LATCH 40373 OCTAL 3ST	!	28462-413N
IC5	ICD BUFF 4503 HEX 3ST	!	28469-179T
L1	IND CHOKE 100UH 10% LAQ		23642-561W

Circuit Ref	Description	Part Number
Unit A1	- KEYBOARD PCB (Contd.)	
MP3	SW CAP RECT O "INCREMENT"	37590-813A
MP4	SW CAP RECT O "STORE"	37590-858G
MP5	SW CAP RECT O "R´CALL"	37590-857F
MP6	SW CAP RECT BN "MOD ALC"	37590-814Z
MP7	SW CAP RECT O "CARR FREQ"	37590-815H
MP8	SW CAP RECT O "FM PM"	37590-816E
MP9	SW CAP RECT O "AM"	37590-817U
MP10	SW CAP RECT O "RF LEVEL"	37590-818Y
MP11	SW CAP RECT BN "7"	37590-819N
MP12	SW CAP RECT BN "4"	37590-820U
MP13	SW CAP RECT BN "1"	37590-821Y
MP14	SW CAP RECT BN "0"	37590-822N
MP15	SW CAP RECT BN "8"	37590-823L
MP16	SW CAP RECT BN "5"	37590-824J
MP17	SW CAP RECT BN "2"	37590-825F
MP18	SW CAP RECT BN "."	37590-826G
MP19	SW CAP RECT BN "6" OR "9"	37590-827V
MP20	SW CAP RECT BN "6" OR "9"	37590-827V
MP21	SW CAP RECT BN "3"	37590-828S
MP22	SW CAP RECT BN "-"	37590-829W
MP23	SW CAP RECT GY "MHZ V"	37590-830V
MP24	SW CAP RECT GY "KHZ MV"	37590-831S
MP25	SW CAP RECT GY "HZ UV"	37590-832W
MP26	SW CAP RECT GY "% RAD DB"	37590-833D
MP27	SW CAP RECT BN "INT EXT"	37590-834T
MP28	SW CAP RECT BN "MOD ON OFF"	37590-835P
MP29	SW CAP RECT BN "TOTAL INCR"	37590-836X
MP30	SW CAP RECT BN "ARROW"	37590-859V
MP31	SW CAP RECT BU "SECOND FUNCT"	37590-837M
MP32	SW CAP RECT BN "CARR ON OFF"	37590-838C
MP33	SW CAP RECT BN "RETURN"	37590-839R
MP34	SW CAP RECT BN "ARROW"	37590-859V
MP35	SPACER (LED)	37590-737R
R1	RES MF 470R 1/4W 2% 100PPM	24773-265M
R2	RV CERM 2K LIN .3W 10% FLAT	25748-505T
R3	RES MF 3K9 1/4W 2% 100PPM	24773-287V
R4	RES MF 100R 1/4W 2% 100PPM	24773-249J
R5	RES MF 470R 1/4W 2% 100PPM	24773-265M
R6	RES MF 10K 1/4W 0.5% 50PPM	24753-628N
R7	RES MF 10K 1/4W 0.5% 50PPM	24753-628N
R8	RES MF 62K 1/4W 2% 100PPM	24773-316Y
R9	RES NET 100K - 5% - 8SIP L/P	24681-635F
R10	RES MF 150R 1/4W 2% 100PPM	24773-253F

Circuit Ref	Description	Part Number
Unit A1	- KEYBOARD PCB (Contd.)	
R11	RES MF 150R 1/4W 2% 100PPM	24773-253F
R12	RES MF 150R 1/4W 2% 100PPM	24773-253F
R13	RES MF 150R 1/4W 2% 100PPM	24773-253F
SA	SW PUSH 1P1W MOM LIPA D6	23465-301P
SB	SW PUSH 1P1W MOM LIPA D6	23465-301P
SC	SW PUSH 1P1W MOM LIPA D6	23465-301P
SD	SW PUSH 1P1W MOM LIPA D6	23465-301P
SE	SW PUSH 1P1W MOM LIPA D6	23465-301P
SF	SW PUSH 1P1W MOM LIPA D6	23465-301P
SG	SW PUSH 1P1W MOM LIPA D6	23465-301P
SH	SW PUSH 1P1W MOM LIPA D6	23465-301P
SJ	SW PUSH 1P1W MOM LIPA D6	23465-301P
SK	SW PUSH 1P1W MOM LIPA D6	23465-301P
SL	SW PUSH 1P1W MOM LIPA D6	23465-301P
SM	SW PUSH 1P1W MOM LIPA D6	23465-301P
SN	SW PUSH 1P1W MOM LIPA D6	23465-301P
SP	SW PUSH 1P1W MOM LIPA D6	23465-301P
SR	SW PUSH 1P1W MOM LIPA D6	23465-301P
SS	SW PUSH 1P1W MOM LIPA D6	23465-301P
ST	SW PUSH 1P1W MOM LIPA D6	23465-301P
SU	SW PUSH 1P1W MOM LIPA D6	23465-301P
SV	SW PUSH 1P1W MOM LIPA D6	23465-301P
SW	SW PUSH 1P1W MOM LIPA D6	23465-301P
SX	SW PUSH 1P1W MOM LIPA D6	23465-301P
SY	SW PUSH 1P1W MOM LIPA D6	23465-301P
SZ	SW PUSH 1P1W MOM LIPA D6	23465-301P
SAA	SW PUSH 1P1W MOM LIPA D6	23465-301P
SAB	SW PUSH 1P1W MOM LIPA D6	23465-301P
SAC	SW PUSH 1P1W MOM LIPA D6	23465-301P
SAD	SW PUSH 1P1W MOM LIPA D6	23465-301P
SAE	SW PUSH 1P1W MOM LIPA D6	23465-301P
SAF	SW PUSH 1P1W MOM LIPA D6	23465-301P
SAG	SW PUSH 1P1W MOM LIPA D6	23465-301P
SAH	SW PUSH 1P1W MOM LIPA D6	23465-301P
SAJ	SW PUSH 1P1W MOM LIPA D6	23465-301P
TR1	TR PSI BC308B 20V 130M - GEN	28433-455R
X1	LIQUID CRYSTAL DISPLAY	44990-490W
X2	CON ELAS - - - 6.35X3.56X119.4	23436-030E

Circuit Ref	Description	Part Number
Unit A2	- POWER SUPPLY & CONTROL PCB	
9.	When ordering, prefix circuit reference with A2	
	Complete unit	44828-784Z
C1	CAP ELEC 15000U 16V -10+30% PC	26422-307Y
C2	CAP ELEC 6800U 25V -10+30% PC	26422-308N
C3	CAP ELEC 220U 25V 20%+ PCB	26421-125V
C4	CAP ELEC 220U 25V 20%+ PCB	26421-125V
C5	CAP ELEC 470U 25V 20%+ PCB	26421-129T
C6	CAP ELEC 100U 50V 20%+ PCB	26421-123F
C7	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C8	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C9	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C10	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C11	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C12	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C13	CAP ELEC 4U7 35V 20% SUBMIN	26421-108A
C14	CAP ELEC 100U 6.3V 20% SUBMIN	26421-118L
C15	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C16	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C17	CAP CER 220P 63V 2% PLATE	26343-481S
C18	CAP PETP 470N 63V 10% RAD MIN	26582-427L
C19	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C20	CAP CER 220P 63V 2% PLATE	26343-481S
C21	CAP PETP 470N 63V 10% RAD MIN	26582-427L
C22	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C23	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C24	CAP PETP 47N 63V 10% RAD MIN	26582-428J
C25	CAP PETP 1U0 50V 10% RAD MIN	26582-432F
C26	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C27	CAP CER 4P7 63V .5PF PLATE	26343-461B
C28	CAP CER 4P7 63V .5PF PLATE	26343-461B
C29	CAP PS 1N5 63V 1% RAD	26538-906D
C30	CAP CER 18P 63V 5% PLATE	26343-468Y
C31	CAP CER 4P7 63V .5PF PLATE	26343-461B
C32	CAP PETP 2U2 63V 10% RAD	26582-418Z
C33	CAP PS 4N7 63V 1% RAD	26538-918A
C34	CAP CER 15P 63V 5% PLATE	26343-467U
C35	CAP CER 47P 63V 5% PLATE	26343-473U
C36	CAP CER 15P 63V 5% PLATE	26343-467U
C37	CAP CER 15P 63V 5% PLATE	26343-467U
C38	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C39	CAP CER 180P 63V 2% PLATE	26343-480V

Circuit Ref	Description	Part Number
Unit A2	- POWER SUPPLY & CONTROL PCB (Contd.)	
C40	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C41	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C42	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C43	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C44	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C45	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C46	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C47	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C48	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C49	CAP CER 1N0 63V 10% PLATE	26383-585M
C50	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C51	CAP ELEC 100U 6.3V 20% SUBMIN	26421-118L
C52	CAP PETP 1U0 50V 10% RAD MIN	26582-432F
C53	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C54	CAP PETP 220N 63V 10% RAD MIN	26582-430L
D1	DI RECT 1N5401 100V	28355-723N
D2	DI RECT 1N5401 100V	28355-723N
D3	DI BRIDGE 2KBB20R 200V 1.9A	28359-189D
D4	DI BRIDGE 2KBB20R 200V 1.9A	28359-189D
D5	DI RECT 1N4004 400V	28357-028K
D6	DI RECT 1N4004 400V	28357-028K
D7	DI RECT 1N4004 400V	28357-028K
D8	DI ZEN 1N825/A 6.2V 5%	28371-494Z
D9	DI SIL 1N4148 75V JUNC	28336-676J
D10	DI ZEN 1N825/A 6.2V 5%	28371-494Z
D11	DI SIL 1N4148 75V JUNC	28336-676J
D12	DI SIL 1N4148 75V JUNC	28336-676J
D13	DI SIL 1N4148 75V JUNC	28336-676J
D14	DI SIL 1N4148 75V JUNC	28336-676J
D15	DI SIL 1N4148 75V JUNC	28336-676J
D16	DI SIL 1N4148 75V JUNC	28336-676J
D17	DI SIL 1N4148 75V JUNC	28336-676J
D18	DI SIL 1N4148 75V JUNC	28336-676J
D19	DI SIL 1N4148 75V JUNC	28336-676J
D20	DI SIL 1N4148 75V JUNC	28336-676J
D21	DI SIL 1N4148 75V JUNC	28336-676J
D22	DI SIL 1N4148 75V JUNC	28336-676J
D23	DI SIL 1N4148 75V JUNC	28336-676J
D24	DI SIL 1N4148 75V JUNC	28336-676J
D25	DI SIL 1N4148 75V JUNC	28336-676J
D26	DI SIL 1N4148 75V JUNC	28336-676J
D27	DI SIL 1N4148 75V JUNC	28336-676J
D28	DI SIL 1N4148 75V JUNC	28336-676J

Circuit Ref	Description		Part Number
Unit A2	- POWER SUPPLY & CONTROL PCB (Contd.)		
IC1	ICA VREG- LM337T PROG 1A5		28461-727Z
IC2	ICA VREG+ LM317T PROG 1A5		28461-726A
IC3	ICA AMP TL072CP DUAL FET I/P		28461-348Z
IC4	ICD BUFF 4049B HEX INV BI	!	28469-162Z
IC5	ICD SH REG 4094 8BIT STR/LA	!	28467-521W
IC6	ICD AND 4081 QUAD 2INP BI	!	28466-009L
IC7	ICD SH REG 4094 8BIT STR/LA	!	28467-521W
IC8	ICD SH REG 4021 8BIT PISO	!	28467-527C
IC9	ICD SH REG 4094 8BIT STR/LA	!	28467-521W
IC10	ICD DEC/DMX 4515 4-16 LATCHED	!	28465-036T
IC11	ICD FF D 40174 HEX	!	28462-616Y
IC12	ICD NAND 4011 QUAD 2INP BI	!	28466-340R
IC13	ICD BUFF 4503 HEX 3ST	!	28469-179T
IC14	ICA MUX 4053 TRIP 3INP	!	28469-714H
IC15	ICA AMP TL074CN QUAD FET I/P		28461-349H
IC16	ICA AMP TL074CN QUAD FET I/P		28461-349H
IC17	ICA AMP TL074CN QUAD FET I/P		28461-349H
IC18	ICA AMP TL074CN QUAD FET I/P		28461-349H
IC19	ICA DAC AD7528JN DUAL 8BIT	!	28469-428C
IC20	ICA DAC AD7528JN DUAL 8BIT	!	28469-428C
IC21	ICA AMP NE5532 DUAL LN DIL8		28461-363G
IC22	ICD FF D 40174 HEX	!	28462-616Y
IC23	ICA DAC AD7528JN DUAL 8BIT	!	28469-428C
IC24	ICA DAC AD7528JN DUAL 8BIT	!	28469-428C
IC25	ICD FF D 40174 HEX	!	28462-616Y
IC26	ICD NAND 4093 QUAD 2INP SCH BI	!	28469-203U
IC27	ICA ARRAY CA3046 5 NPN TRAN		28461-901A
L1	IND CHOKE 100UH 10% LAQ		23642-561W
R1	RES MF 750R 1/4W 2% 100PPM		24773-270R
R2	RES MF 220R 1/4W 2% 100PPM		24773-257W
R3	RES MO 51R 1/2W 2% 250PPM		24573-042D
R4	RES MF 220R 1/4W 2% 100PPM		24773-257W

Circuit Ref	Description	Part Number
Unit A2	- POWER SUPPLY & CONTROL PCB (Contd.)	
R5	RV CERM 50R LIN .5W 10% HORZ	25711-634N
R6	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R7	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R8	RV CERM 50R LIN .5W 10% HORZ	25711-634N
R9	RES MF 220R 1/4W 2% 100PPM	24773-257W
R10	RES MF 680R 1/4W 2% 100PPM	24773-269K
R11	RES MF 680R 1/4W 2% 100PPM	24773-269K
R12	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R13	RES MF 620R 1/4W 2% 100PPM	24773-268B
R14	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R15	RV CERM 2KO LIN .5W 10% HORZ	25711-639V
R16	RES MF 16K 1/4W 2% 100PPM	24773-302X
R17	RES MF 560R 1/4W 2% 100PPM	24773-267R
R18	RES MF 100K 1/4W 2% 100PPM	24773-321L
R19	RES WW 0R1 1.5W 10%	25133-032C
R20	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R21	RES MF 10K 1/4W 2% 100PPM	24773-297M
R22	RES MF 10K 1/4W 2% 100PPM	24773-297M
R23	RES MF 100R 1/4W 2% 100PPM	24773-249J
R24	RES MF 100K 1/4W 2% 100PPM	24773-321L
R25	RES MF 100K 1/4W 2% 100PPM	24773-321L
R26	RES MF 10K 1/4W 2% 100PPM	24773-297M
R27	RES MF 10K 1/4W 2% 100PPM	24773-297M
R28	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R29	RES MF 560R 1/4W 2% 100PPM	24773-267R
R30	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R31	RES MF 10K 1/4W 2% 100PPM	24773-297M
R32	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R33	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R34	RES MF 100K 1/4W 2% 100PPM	24773-321L
R35	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R36	RES MF 360R 1/4W 2% 100PPM	24773-262T
R37	RES MF 360R 1/4W 2% 100PPM	24773-262T
R38	RES MF 4K3 1/4W 2% 100PPM	24773-288S
R39	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R40	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R41	RES MF 10K 1/4W 2% 100PPM	24773-297M
R42	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R43	RES MF 220K 1/4W 2% 100PPM	24773-329T
R44	RES MF 240K 1/4W 2% 100PPM	24773-330W
R45	RES MF 560K 1/4W 2% 100PPM	24773-340R
R46	RES MF 100K 1/4W 2% 100PPM	24773-321L

Circuit Ref	Description	Part Number
Unit A2	- POWER SUPPLY & CONTROL PCB (Contd.)	
R47	RES MF 100K 1/4W 2% 100PPM	24773-321L
R48	RES MF 100K 1/4W 2% 100PPM	24773-321L
R49	RES MF 100K 1/4W 2% 100PPM	24773-321L
R50	RES MF 10KO 1/4W 0.1% 15PPM	24723-373P
R51	RES MF 1K8 1/4W .1% 25PPM	24753-597G
R52	RES MF 10KO 1/4W 0.1% 15PPM	24723-373P
R53	RES MF 18K 1/4W 0.1% 25 PPM	24753-344K
R54	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R55	RES MF 18K 1/4W 2% 100PPM	24773-303M
R56	RV CERM 2KO LIN .5W 10% HORZ	25711-639V
R57	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R58	RV CERM 1KO LIN .5W 10% HORZ	25711-638G
R59	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R60	RES MF 10K 1/4W 2% 100PPM	24773-297M
R61	RES MF 100R 1/4W 2% 100PPM	24773-249J
R62	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R63	RES MF 820K 1/4W 2% 100PPM	24773-344Z
R64	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R65	RES MF 150R 1/4W 2% 100PPM	24773-253F
R66	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R67	RV CERM 1KO LIN .5W 10% HORZ	25711-638G
R68	RES MF 1K6 1/4W 2% 100PPM	24773-278Y
R69	RES MF 13K 1/4W 2% 100PPM	24773-300T
R70	RES MF 47K 1/4W 2% 100PPM	24773-313H
R71	RES MF 390K 1/4W 2% 100PPM	24773-335M
R72	RES MF 10K 1/4W 2% 100PPM	24773-297M
R73	RES MF 18K 1/4W 2% 100PPM	24773-303M
R74	RES MF 15K 1/4W 2% 100PPM	24773-301P
R75	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R76	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R77	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R78	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R79	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R80	RES MF 39K 1/4W 2% 100PPM	24773-311A
R81	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R82	RES MF 15K 1/4W 2% 100PPM	24773-301P
R83	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R84	RV CERM 100K LIN .5W 10% HORZ	25711-644W
R85	RES MF 100R 1/4W 2% 100PPM	24773-249J
R86	RES MF 620R 1/4W 2% 100PPM	24773-268B
R87	RES MF 12K 1/4W 2% 100PPM	24773-299R
R88	RES MF 100K 1/4W 2% 100PPM	24773-321L
R89	RV CERM 100R LIN .5W 10% HORZ	25711-635L

Circuit Ref	Description	Part Number
Unit A2	- POWER SUPPLY & CONTROL PCB (Contd.)	
R90	RV CERM 100K LIN .5W 10% HORZ	25711-644W
R91	RES MF 560R 1/4W 2% 100PPM	24773-267R
R92	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R93	RES MF 220K 1/4W 2% 100PPM	24773-329T
R94	RES MF 100K 1/4W 2% 100PPM	24773-321L
R95	RES MF 330R 1/4W 2% 100PPM	24773-261D
R96	RES MF 330R 1/4W 2% 100PPM	24773-261D
R97	RES MF 100K 1/4W 2% 100PPM	24773-321L
R98	RES MF 100K 1/4W 2% 100PPM	24773-321L
R99	RES MF 100K 1/4W 2% 100PPM	24773-321L
R100	RES MF 22K 1/4W 2% 100PPM	24773-305R
R101	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R102	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R103	RES MF 470R 1/4W 2% 100PPM	24773-265M
R104	RES MF 100K 1/4W 2% 100PPM	24773-321L
R105	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R107	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R108	RES WW 10R 1.5W 5%	25123-020F
R111	RES MF 150R 1/4W 2% 100PPM	24773-253F
R112	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R113	RV CERM 1KO LIN .5W 10% HORZ	25711-638G
RLA	RELAY REED 1NO 5V 500R	23486-442F
TR1	TR NSI BC108A&B 20V 150M - GEN	28452-787N
TR3	TR NSI BC208B 20V 150M - GEN	28452-781A
TR4	TR NSI BC208B 20V 150M - GEN	28452-781A
TR5	TR NSI BC208B 20V 150M - GEN	28452-781A
TR6	TR NSI BC208B 20V 150M - GEN	28452-781A
TR7	TR NJF J310 25V - 24MA	28459-028E
TR8	TR PSI BC308B 20V 130M - GEN	28433-455R
TR9	TR PSI BC308B 20V 130M - GEN	28433-455R
TR10	TR PSI BC308B 20V 130M - GEN	28433-455R
TR11	TR PSI BC308B 20V 130M - GEN	28433-455R
TR12	TR PSI BC308B 20V 130M - GEN	28433-455R
TR13	TR PSI BC308B 20V 130M - GEN	28433-455R
TR16	TR PSI BC308B 20V 130M - GEN	28433-455R

Circuit Ref	Description	Part Number
Unit AA0	- RF BOX ASSY A	
10. When ordering, prefix circuit reference with AA0		
	Complete unit	44990-446L
C1	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C2	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C3	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C4	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C5	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C6	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C7	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C8	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C9	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C10	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C11	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C12	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C13	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C14	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C15	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C16	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C17	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C18	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C19	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C20	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C21	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C22	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C23	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C24	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C25	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C26	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C27	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C28	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C29	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C30	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C31	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C32	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C33	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
C34	CAP CER 1NO 300V 20%+ L/T SOL	26373-733K
L1	IND CHOKE 5 TURNS	44190-036B
L2	IND CHOKE 5 TURNS	44190-036B
L3	IND CHOKE 5 TURNS	44190-036B
L4	IND CHOKE 5 TURNS	44190-036B

Circuit Ref	Description	Part Number
Unit AA0	- RF BOX ASSY A	(Contd.)
L6	IND CHOKE 5 TURNS	44190-036B
L7	IND CHOKE 5 TURNS	44190-036B
L8	IND CHOKE 5 TURNS	44190-036B
L9	IND CHOKE 5 TURNS	44190-036B
L10	IND CHOKE 5 TURNS	44190-036B
L11	IND CHOKE 5 TURNS	44190-036B
L12	IND CHOKE 2.5 TURNS	44190-909X
L13	IND CHOKE 2.5 TURNS	44190-909X
L14	IND CHOKE 2.5 TURNS	44190-909X
L15	IND CHOKE 2.5 TURNS	44190-909X
L16	IND CHOKE 2.5 TURNS	23642-909X
L17	IND CHOKE 2.5 TURNS	23642-909X
L18	IND CHOKE 2.5 TURNS	23642-909X
X7	FERRITE BEAD	41372-006T
X8	FERRITE BEAD	41372-006T
X9	FERRITE BEAD	41372-006T
X10	FERRITE BEAD	41372-006T
X11	FERRITE BEAD	41372-006T
X12	FERRITE BEAD	41372-006T
X13	FERRITE BEAD	41372-006T
X14	FERRITE BEAD	41372-006T
X15	FERRITE BEAD	41372-006T
X16	FERRITE BEAD	41372-006T
X17	FERRITE BEAD	41372-006T
X18	FERRITE BEAD	41372-006T
X19	FERRITE BEAD	41372-006T
X20	FERRITE BEAD	41372-006T
X21	FERRITE BEAD	41372-006T
X22	FERRITE BEAD	41372-006T
X23	FERRITE BEAD	41372-006T
X24	FERRITE BEAD	41372-006T
X25	FERRITE BEAD	41372-006T
X26	FERRITE BEAD	41372-006T
Unit AA1	- SYNTHESIZER PCB	
11. When ordering, prefix circuit reference with AA1		
	Complete unit	44828-786E
C1	CAP CER 1NO 63V 10% PLATE	26383-585M
C2	CAP CER 1NO 63V 10% PLATE	26383-585M
C3	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C4	CAP CER 1NO 63V 10% PLATE	26383-585M
C5	CAP CER 1NO 63V 10% PLATE	26383-585M

Circuit Ref	Description	Part Number
Unit AA1	- SYNTHESIZER PCB	(Contd.)
C6	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C7	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C8	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C9	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C10	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C11	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C12	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C13	CAP CER 1N0 63V 10% PLATE	26383-585M
C14	CAP CER 1N0 63V 10% PLATE	26383-585M
C15	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C16	CAP CER 100P 63V 2% PLATE	26343-477V
C17	CAP PS 1N0 63V 1% RAD	26538-902G
C18	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C19	CAP PETP 10N 63V 2.5% RAD MIN	26582-494L
C20	CAP PETP 4N7 63V 2.5% RAD MIN	26582-493N
C21	CAP PETP 10N 63V 2.5% RAD MIN	26582-494L
C22	CAP CER 270P 63V 2% PLATE	26343-483D
C23	CAP CER 1N0 63V 10% PLATE	26383-585M
C24	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C25	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C26	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C27	CAP PETP 1U0 50V 10% RAD MIN	26582-432F
C28	CAP CER 1N0 63V 10% PLATE	26383-585M
C29	CAP CER 1N0 63V 10% PLATE	26383-585M
C30	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C31	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C32	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C33	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C34	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C35	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C36	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C37	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C38	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C39	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C40	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C41	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C42	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C43	CAP PETP 1U0 50V 10% RAD MIN	26582-432F
C44	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C45	CAP CER 10N 50V 20% X7R MON AX	26346-120Y

Circuit Ref	Description		Part Number
Unit AA1	- SYNTHESIZER PCB		(Contd.)
C46	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C47	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C48	CAP CER 10P 63V .5PF PLATE		26343-465H
C49	CAP CER 220P 63V 2% PLATE		26343-481S
C50	CAP PS 150P 63V 2% RAD		26538-571R
C51	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C52	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C53	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C54	CAP PETP 1U0 50V 10% RAD MIN		26582-432F
C55	CAP ELEC 1000U 6V 20%+ PCB		26421-128D
C56	CAP CER 4P7 63V .5PF PLATE		26343-461B
C57	CAP PETP 100N 63V 10% RAD MIN		26582-429F
C58	CAP ELEC 10U 35V 20% SUBMIN		26421-112Z
C59	CAP ELEC 10U 35V 20% SUBMIN		26421-112Z
C60	CAP ELEC 10U 35V 20% SUBMIN		26421-112Z
C61	CAP ELEC 10U 35V 20% SUBMIN		26421-112Z
D1	DI SIL 1N4148 75V JUNC		28336-676J
D2	DI SIL 1N4148 75V JUNC		28336-676J
D3	DI SIL 1N4148 75V JUNC		28336-676J
D4	DI SIL 1N4148 75V JUNC		28336-676J
D5	DI SIL 1N4148 75V JUNC		28336-676J
D6	DI SIL 1N4148 75V JUNC		28336-676J
D7	DI SIL 1N4148 75V JUNC		28336-676J
D8	DI SIL 1N4148 75V JUNC		28336-676J
D9	DI SIL 1N4148 75V JUNC		28336-676J
D10	DI ZEN BZX79C5V1 5.1V 5%		28371-401U
D11	DI SIL 1N4148 75V JUNC		28336-676J
D12	DI SIL 1N4148 75V JUNC		28336-676J
IC1	ICD DIV SP8659B /16 200MHZ		28469-429R
IC2	ICD NAND 74S00N QUAD 2INP		28466-331D
IC3	ICD FF D 40174 HEX	!	28462-616Y
IC4	ICD CTR 74LS191 4BIT BIN U/D		28464-022X
IC5	ICD CTR 74LS191 4BIT BIN U/D		28464-022X
IC6	ICD FF D 74S74 DUAL +EDG TR		28462-607K
IC7	ICD FF D 74S74 DUAL +EDG TR		28462-607K
IC8	ICD CTR 74LS390 DUAL 4BIT DEC		28464-127R
IC9	ICD DIV SP8906 4MOD PRESCALER		28469-430M
IC10	ICD NAND 74LS00 QUAD 2INP		28466-345H
IC11	ICD FF D 74LS74 DUAL +EDG TR		28462-611A
IC12	ICA AMP TL074CN QUAD FET I/P		28461-349H
IC13	ICD FF D 40174 HEX	!	28462-616Y

Circuit Ref	Description		Part Number
Unit AA1	- SYNTHESIZER PCB (Contd.)		
IC14	ICD CTR 74LS390 DUAL 4BIT DEC		28464-127R
IC15	ICD NAND 74LS00 QUAD 2INP		28466-345H
IC16	ICD CTR 74LS191 4BIT BIN U/D		28464-022X
IC17	ICD CTR 74LS191 4BIT BIN U/D		28464-022X
IC18	ICA COMP LM311N DIL8		28461-695U
IC19	ICD FF D 40174 HEX	!	28462-616Y
IC20	ICD NAND 74LS00 QUAD 2INP		28466-345H
IC21	ICA AMP TL072CP DUAL FET I/P		28461-348Z
IC22	ICD FF D 74LS74 DUAL +EDG TR		28462-611A
IC23	ICD FF D 40174 HEX	!	28462-616Y
IC24	ICD FF D 40174 HEX	!	28462-616Y
IC25	ICD ADDER 4008 4BIT FULL	!	28469-363B
IC26	ICD ADDER 4008 4BIT FULL	!	28469-363B
IC27	ICD ADDER 4008 4BIT FULL	!	28469-363B
IC28	ICA AMP TL071CP FET I/P DIL8		28461-347A
IC29	ICD ADDER 4008 4BIT FULL	!	28469-363B
IC30	ICD ADDER 4008 4BIT FULL	!	28469-363B
IC31	ICD FF D 40174 HEX	!	28462-616Y
IC32	ICD FF D 40174 HEX	!	28462-616Y
IC33	ICA DAC AD7524JN 8BIT	!	28469-400R
IC34	ICD NAND 74LS132 QUAD 2INP SCH		28469-205N
L1	IND CHOKE 100UH 10% LAQ		23642-561W
L2	IND CHOKE 1000UH 10% LAQ		23642-567C
L3	IND CHOKE 1.0UH 10% LAQ		23642-549L
L4	IND CHOKE 1000UH 10% LAQ		23642-567C
R1	RES MF 33K 1/4W 2% 100PPM		24773-309Z
R2	RES MF 51R 1/4W 2% 100PPM		24773-242Z
R3	RES MF 470R 1/4W 2% 100PPM		24773-265M
R4	RES MF 470R 1/4W 2% 100PPM		24773-265M
R5	RES MF 150R 1/4W 2% 100PPM		24773-253F
R6	RES MF 51R 1/4W 2% 100PPM		24773-242Z
R7	RES MF 470R 1/4W 2% 100PPM		24773-265M
R8	RES MF 470R 1/4W 2% 100PPM		24773-265M
R9	RES MF 470R 1/4W 2% 100PPM		24773-265M
R10	RES MF 470R 1/4W 2% 100PPM		24773-265M
R11	RES MF 39K 1/4W 2% 100PPM		24773-311A
R12	RES MF 22K 1/4W 2% 100PPM		24773-305R
R13	RES MF 100K 1/4W 2% 100PPM		24773-321L
R14	RES MF 10K 1/4W 2% 100PPM		24773-297M
R15	RES MF 100K 1/4W 2% 100PPM		24773-321L
R16	RES MF 2K2 1/4W 2% 100PPM		24773-281Y
R17	RES MF 1K0 1/4W 2% 100PPM		24773-273A
R18	RES MF 2K2 1/4W 2% 100PPM		24773-281Y

Circuit Ref	Description	Part Number
Unit AA1	- SYNTHESIZER PCB (Contd.)	
R19	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R20	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R21	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R22	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R23	RES MF 36K 1/4W 2% 100PPM	24773-310K
R24	RES MF 36K 1/4W 2% 100PPM	24773-310K
R25	RES MF 100K 1/4W 2% 100PPM	24773-321L
R26	RES MF 62K 1/4W 2% 100PPM	24773-316Y
R27	RES MF 100R 1/4W 2% 100PPM	24773-249J
R28	RES MF 470R 1/4W 2% 100PPM	24773-265M
R29	RES MF 1K8 1/4W 2% 100PPM	24773-279N
R30	RES MF 470R 1/4W 2% 100PPM	24773-265M
R31	RES MF 1K8 1/4W 2% 100PPM	24773-279N
R32	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R33	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R34	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R35	RES MF 100K 1/4W 2% 100PPM	24773-321L
R36	RES MF 10K 1/4W 2% 100PPM	24773-297M
R37	RES MF 18K 1/4W 2% 100PPM	24773-303M
R38	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R39	RES MF 470R 1/4W 2% 100PPM	24773-265M
R40	RES MF 470R 1/4W 2% 100PPM	24773-265M
R41	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R42	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R43	RV CERM 2K0 LIN .5W 10% HORZ	25711-639V
R44	RES MF 100R 1/4W 2% 100PPM	24773-249J
R45	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R46	RES MF 16K 1/4W 2% 100PPM	24773-302X
R47	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R48	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R49	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R50	RES MF 100R 1/4W 2% 100PPM	24773-249J
R51	RES MF 100R 1/4W 2% 100PPM	24773-249J
TR1	TR NSI BC208B 20V 150M - GEN	28452-781A
TR2	TR PSI BC308B 20V 130M - GEN	28433-455R
TR3	TR NSI BC208B 20V 150M - GEN	28452-781A
TR4	TR PSI BC308B 20V 130M - GEN	28433-455R
TR5	TR PSI BC308B 20V 130M - GEN	28433-455R
TR6	TR NSI 2N2369 15V 500M - SW	28452-197H
TR7	TR NSI BC208B 20V 150M - GEN	28452-781A

Circuit Ref	Description		Part Number
Unit AA1	- SYNTHESIZER PCB (Contd.)		
TR8	TR PSI BC308B 20V 130M - GEN		28433-455R
TR9	TR NSI 2N2369 15V 500M - SW		28452-197H
TR10	TR PSI BC308B 20V 130M - GEN		28433-455R
X1	OSC 10MHZ (HS OVEN)		44990-418V
Unit AA2	- MICROPROCESSOR PCB		
12. When ordering, prefix circuit reference with AA2			
	Complete unit		44828-787U
C3	CAP ELEC 4U7 35V 20% SUBMIN		26421-108A
C5	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C6	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C7	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C8	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C9	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C10	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C11	CAP PETP 100N 63V 10% RAD MIN		26582-429F
C12	CAP PETP 100N 63V 10% RAD MIN		26582-429F
C13	CAP PETP 100N 63V 10% RAD MIN		26582-429F
C14	CAP PETP 100N 63V 10% RAD MIN		26582-429F
C15	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C16	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C17	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C18	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C19	CAP ELEC 47U 63V 20%+ PCB		26421-121L
C20	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
D2	DI ZEN 1N825/A 6.2V 5%		28371-494Z
D6	DI SIL 1N4148 75V JUNC		28336-676J
IC1	ICA AMP TL071CP DUAL FET I/P		28461-347P
IC2	ICD MP P8085A 8BIT NMOS	!	28469-396K
IC3	ICD LATCH 74LS373 OCT 3ST		28462-410E
IC4	ICD DEC/DMX 74LS138 3-8		28465-027F
IC5	ICD PROM		
IC6	ICD PROM Set of 4	!	44533-113J
IC7	ICD PROM		
IC8	ICD PROM		
IC9	ICD RAM HM6116P-4 2KX8 200NS	!	28469-307N
IC10	ICD PROM 2817A-2 2KX8 EA DIL28	!	28471-025D
IC11	ICD DEC/DMX 74LS138 3-8		28465-027F

Circuit Ref	Description		Part Number
Unit AA2	- MICROPROCESSOR PCB (Contd.)		
IC12	ICD OR 74LS32 QUAD 2INP		28466-108U
IC13	ICD BUFF 74LS125A QUAD 3ST		28469-184X
IC14	ICD FF D 74LS175 QUAD +EDG TR		28462-614E
IC15	ICD FF D 40174 HEX	!	28462-616Y
IC16	ICD FF D 40174 HEX	!	28462-616Y
IC17	ICD CTR 74LS393 DUAL 4BIT BIN		28464-130R
IC18	ICD DIV 4020 14STAGE	!	28464-107N
R1	RV CERM 1KO LIN .5W 10% HORZ		25711-638G
R2	RES MF 3K9 1/4W 2% 100PPM		24773-287V
R3	RES MF 3KO 1/4W 2% 100PPM		24773-284J
R8	RES MF 4K7 1/4W 2% 100PPM		24773-289W
R9	RES MF 4K7 1/4W 2% 100PPM		24773-289W
R10	RES MF 1KO 1/4W 2% 100PPM		24773-273A
R11	RES MF 150K 1/4W 2% 100PPM		24773-325V
R12	RES MF 1KO 1/4W 2% 100PPM		24773-273A
R13	RES MF 10K 1/4W 2% 100PPM		24773-297M
R14	RES MF 10K 1/4W 2% 100PPM		24773-297M
R16	RES MF 10K 1/4W 2% 100PPM		24773-297M
R17	RES MF 1KO 1/4W 2% 100PPM		24773-273A
R18	RES MF 3KO 1/4W 2% 100PPM		24773-284J
R19	RES MF 3KO 1/4W 2% 100PPM		24773-284J
TR2	TR NSI BC208B 20V 150M - GEN		28452-781A

Unit AB0 - RF BOX ASSY B

13. When ordering, prefix circuit reference with AB0

	Complete unit		44990-447J
C1	CAP CER 1N0 300V 20%+ L/T SOL		26373-733K
C2	CAP CER 1N0 300V 20%+ L/T SOL		26373-733K
C3	CAP CER 1N0 300V 20%+ L/T SOL		26373-733K
C4	CAP CER 1N0 300V 20%+ L/T SOL		26373-733K
C5	CAP CER 1N0 300V 20%+ L/T SOL		26373-733K

Circuit Ref	Description	Part Number
Unit A80	- RF BOX ASSY B	(Contd.)
C6	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C7	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C8	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C9	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C10	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C11	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C12	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C13	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C14	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C15	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C16	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C17	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C18	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C19	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C20	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C21	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C22	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C23	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C24	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C25	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C26	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C27	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C28	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C29	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
C30	CAP CER 1N0 300V 20%+ L/T SOL	26373-733K
L1	IND CHOKE 5 TURNS	44190-036B
L2	IND CHOKE 5 TURNS	44190-036B
L3	IND CHOKE 5 TURNS	44190-036B
L4	IND CHOKE 5 TURNS	44190-036B
L5	IND CHOKE 5 TURNS	44190-036B
L6	IND CHOKE 5 TURNS	44190-036B
L7	IND CHOKE 5 TURNS	44190-036B
L8	IND CHOKE 5 TURNS	44190-036B
L9	IND CHOKE 5 TURNS	44190-036B
L10	IND CHOKE 5 TURNS	44190-036B
L11	IND CHOKE 5 TURNS	44190-036B
L12	IND CHOKE 5 TURNS	44190-036B
L13	IND CHOKE 2.5 TURNS	23642-909X
L14	IND CHOKE 2.5 TURNS	23642-990X
L15	IND CHOKE 2.5 TURNS	23642-990X
X4	FERRITE BEAD	41372-006T
X5	FERRITE BEAD	41372-006T
X6	FERRITE BEAD	41372-006T
X7	FERRITE BEAD	41372-006T

Circuit Ref	Description	Part Number
Unit AB0	- RF BOX ASSY B	(Contd.)
X8	FERRITE BEAD	41372-006T
X9	FERRITE BEAD	41372-006T
X10	FERRITE BEAD	41372-006T
X11	FERRITE BEAD	41372-006T
X12	FERRITE BEAD	41372-006T
X13	FERRITE BEAD	41372-006T
X14	FERRITE BEAD	41372-006T
X15	FERRITE BEAD	41372-006T
X16	FERRITE BEAD	41372-006T
X17	FERRITE BEAD	41372-006T
X18	FERRITE BEAD	41372-006T
X19	FERRITE BEAD	41372-006T
Unit AB1	- RF PROCESSING PCB	
14. When ordering, prefix circuit reference with AB1		
	Complete unit	44828-788Y
C1	CAP ELEC 220U 10V 20%+ AX	26415-817J
C2	CAP CER 220P 63V 10% PLATE	26383-595H
C3	CAP CER 10P 50V 10% NPO MON	26343-570H
C4	CAP CER 22P 50V 10% NPO MON	26343-572U
C5	CAP CER 220P 63V 10% PLATE	26383-595H
C6	CAP TANT 10U 35V 20% BEAD	26486-225C
C7	CAP VAR PLAS 22P 2P TRIM	26878-407U
C8	CAP CER 220P 63V 10% PLATE	26383-595H
C9	CAP CER 220P 63V 10% PLATE	26383-595H
C10	CAP CER 220P 63V 10% PLATE	26383-595H
C11	CAP CER 220P 63V 10% PLATE	26383-595H
C12	CAP TANT 1U0 35V 20% BEAD	26486-209F
C13	CAP CER 220P 63V 10% PLATE	26383-595H
C14	CAP CER 220P 63V 10% PLATE	26383-595H
C15	CAP CER 33P 63V 5% PLATE	26343-471Y
C16	CAP CER 220P 63V 10% PLATE	26383-595H
C17	CAP CER 220P 63V 10% PLATE	26383-595H
C18	CAP VAR PLAS 65P 5P5 TRIM	26878-408Y
C19	CAP CER 220P 63V 10% PLATE	26383-595H
C20	CAP CER 18P 63V 5% PLATE	26343-468Y
C21	CAP CER 220P 63V 10% PLATE	26383-595H
C22	CAP CER 220P 63V 10% PLATE	26383-595H
C23	CAP CER 220P 63V 10% PLATE	26383-595H
C24	CAP CER 33P 63V 5% PLATE	26343-471Y
C25	CAP CER 47P 63V 5% PLATE	26343-473L

Circuit Ref	Description	Part Number
Unit AB1	- RF PROCESSING PCB	(Contd.)
C26	CAP CER 33P 63V 5% PLATE	26343-471Y
C27	CAP PC 1N0 100V 5%	26531-107L
C28	CAP PC 1N0 100V 5%	26531-107L
C29	CAP PC 1N0 100V 5%	26531-107L
C30	CAP CER 220P 63V 10% PLATE	26383-595H
C31	CAP VAR PLAS 22P 2P TRIM	26878-407U
C32	CAP ELEC 220U 10V 20%+ AX	26415-817J
C33	CAP CER 15P 50V 10% NPO MON	26343-571E
C34	CAP CER 15P 50V 10% NPO MON	26343-571E
C35	CAP ELEC 220U 16V 20%+ PCB	26421-124G
C36	CAP CER 220P 63V 10% PLATE	26383-595H
C37	CAP CER 220P 63V 10% PLATE	26383-595H
C38	CAP VAR PLAS 65P 5P5 TRIM	26878-408Y
C39	CAP ELEC 220U 10V 20%+ AX	26415-817J
C40	CAP CER 33P 50V 10% NPO MON	26343-573Y
C41	CAP CER 33P 50V 10% NPO MON	26343-573Y
C42	CAP ELEC 220U 16V 20%+ PCB	26421-124G
C43	CAP CER 220P 63V 10% PLATE	26383-595H
C44	CAP CER 220P 63V 10% PLATE	26383-595H
C45	CAP CER 220P 63V 10% PLATE	26383-595H
C46	CAP CER 220P 63V 10% PLATE	26383-595H
C47	CAP CER 220P 63V 10% PLATE	26383-595H
C48	CAP CER 1N0 63V 10% PLATE	26383-585M
C49	CAP CER 220P 63V 10% PLATE	26383-595H
C50	CAP CER 220P 63V 10% PLATE	26383-595H
C51	CAP CER 220P 63V 10% PLATE	26383-595H
C52	CAP CER 220P 63V 10% PLATE	26383-595H
C53	CAP CER 220P 63V 10% PLATE	26383-595H
C54	CAP CER 220P 63V 10% PLATE	26383-595H
C55	CAP CER 220P 63V 10% PLATE	26383-595H
C56	CAP CER 220P 63V 10% PLATE	26383-595H
C57	CAP CER 220P 63V 10% PLATE	26383-595H
C58	CAP CER 15P 63V 5% PLATE	26343-467U
C59	CAP CER 1N0 63V 10% PLATE	26383-585M
C60	CAP CER 5P6 63V .5PF PLATE	26343-462K
C61	CAP CER 8P2 63V .5PF PLATE	26343-464Z
C62	CAP CER 6P8 63V .5PF PLATE	26343-463A
C63	CAP CER 15P 63V 5% PLATE	26343-467U
C64	CAP CER 10P 63V .5PF PLATE	26343-465H
C65	CAP CER 18P 63V 5% PLATE	26343-468Y
C66	CAP CER 2P7 63V .5PF PLATE	26343-458B
C67	CAP CER 10P 63V .5PF PLATE	26343-465H
C68	CAP CER 1N0 63V 10% PLATE	26383-585M
C69	CAP CER 1N0 63V 10% PLATE	26383-585M

Circuit Ref	Description	Part Number
Unit AB1	- RF PROCESSING PCB (Contd.)	
C70	CAP CER 1N0 63V 10% PLATE	26383-585M
C71	CAP CER 1N0 63V 10% PLATE	26383-585M
C72	CAP CER 3P9 63V .5PF PLATE	26343-460R
C73	CAP CER 12P 63V 5% PLATE	26343-466E
C74	CAP CER 220P 63V 10% PLATE	26383-595H
C75	CAP CER 1N0 63V 10% PLATE	26383-585M
C76	CAP CER 1N0 63V 10% PLATE	26383-585M
C77	CAP CER 1N0 63V 10% PLATE	26383-585M
C78	CAP CER 2P7 63V .5PF PLATE	26343-458B
C79	CAP CER 22P 63V 5% PLATE	26343-469N
C80	CAP CER 220P 63V 10% PLATE	26383-595H
C81	CAP CER 1N0 63V 10% PLATE	26383-585M
C82	CAP CER 220P 63V 10% PLATE	26383-595H
C83	CAP CER 15P 63V 5% PLATE	26343-467U
C84	CAP CER 10N 25V 20% DISC	26383-006C
C85	CAP CER 220P 63V 10% PLATE	26383-595H
C86	CAP CER 33P 63V 5% PLATE	26343-471Y
C87	CAP CER 22P 63V 5% PLATE	26343-469N
C88	CAP CER 22P 63V 5% PLATE	26343-469N
C89	CAP CER 33P 63V 5% PLATE	26343-471Y
C90	CAP CER 5P6 63V .5PF PLATE	26343-462K
C91	CAP CER 68P 63V 2% PLATE	26343-475F
C92	CAP CER 68P 63V 2% PLATE	26343-475F
C93	CAP CER 68P 63V 2% PLATE	26343-475F
C94	CAP TANT 1U0 35V 20% BEAD	26486-209F
C95	CAP CER 1N0 63V 10% PLATE	26383-585M
C96	CAP CER 4P7 63V .5PF PLATE	26343-461B
C97	CAP CER 220P 63V 10% PLATE	26383-595H
C98	CAP CER 220P 63V 10% PLATE	26383-595H
C99	CAP TANT 1U0 35V 20% BEAD	26486-209F
C100	CAP CER 47P 63V 5% PLATE	26343-473L
C101	CAP CER 1N0 63V 10% PLATE	26383-585M
C102	CAP CER 1N0 63V 10% PLATE	26383-585M
C103	CAP CER 220P 63V 10% PLATE	26383-595H
C104	CAP PETP 22N 63V 10% RAD MIN	26582-431J
C105	CAP TANT 10U 35V 20% BEAD	26486-225C
C106	CAP PETP 47N 63V 10% RAD MIN	26582-428J
C107	CAP CER 220P 63V 10% PLATE	26383-595H
C108	CAP CER 1N0 63V 10% PLATE	26383-585M
C109	CAP CER 1N0 63V 10% PLATE	26383-585M
C110	CAP PETP 47N 63V 10% RAD MIN	26582-428J
C111	CAP CER 100P 63V 2% PLATE	26343-477V
C112	CAP CER 1N0 63V 10% PLATE	26383-585M

Circuit Ref	Description	Part Number
Unit AB1	- RF PROCESSING PCB (Contd.)	
C113	CAP CER 47P 63V 5% PLATE	26343-473L
C114	CAP CER 100P 63V 2% PLATE	26343-477V
C115	CAP CER 33P 63V 5% PLATE	26343-494K
C116	CAP PETP 47N 63V 10% RAD MIN	26582-428J
C117	CAP CER 220P 63V 10% PLATE	26383-595H
C118	CAP CER 220P 63V 10% PLATE	26383-595H
C119	CAP CER 220P 63V 10% PLATE	26383-595H
C120	CAP CER 220P 63V 10% PLATE	26383-595H
C121	CAP CER 220P 63V 10% PLATE	26383-595H
C122	CAP CER 220P 63V 10% PLATE	26383-595H
C123	CAP CER 220P 63V 10% PLATE	26383-595H
C124	CAP CER 220P 63V 10% PLATE	26383-595H
C125	CAP CER 220P 63V 10% PLATE	26383-595H
C126	CAP CER 220P 63V 10% PLATE	26383-595H
C127	CAP CER 220P 63V 10% PLATE	26383-595H
C128	CAP CER 39P 63V 5% PLATE	26343-472N
C129	CAP CER 220P 63V 10% PLATE	26383-595H
C130	CAP CER 220P 63V 10% PLATE	26383-595H
C131	CAP CER 220P 63V 10% PLATE	26383-595H
C132	CAP CER 220P 63V 10% PLATE	26383-595H
C134	CAP CER 39P 63V 5% PLATE	26343-472N
C135	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C136	CAP CER 220P 63V 10% PLATE	26383-595H
C137	CAP CER 1N0 63V 10% PLATE	26383-585M
C138	CAP CER 220P 63V 10% PLATE	26383-595H
C139	CAP CER 220P 63V 10% PLATE	26383-595H
C140	CAP CER 220P 63V 10% PLATE	26383-595H
C141	CAP CER 220P 63V 10% PLATE	26383-595H
C142	CAP CER 1N0 63V 10% PLATE	26383-585M
C143	CAP PC 1N0 100V 5%	26531-107L
C144	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C145	CAP CER 220P 63V 10% PLATE	26383-595H
C146	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C147	CAP CER 220P 63V 10% PLATE	26383-595H
C148	CAP CER 4P7 63V .5PF PLATE	26343-461B
C149	CAP CER 22P 63V 5% PLATE	26343-469N
C150	CAP CER 220P 63V 10% PLATE	26383-595H
C151	CAP CER 220P 63V 10% PLATE	26383-595H
C152	CAP CER 220P 63V 10% PLATE	26383-595H
C153	CAP CER 220P 63V 10% PLATE	26383-595H
C154	CAP CER 220P 63V 10% PLATE	26383-595H
C155	CAP CER 220P 63V 10% PLATE	26383-595H
C156	CAP ELEC 33U 25V 20% SUBMIN	26421-115U

Circuit Ref	Description			Part Number
Unit AB1	- RF PROCESSING PCB		(Contd.)	
D1	DI V/CAP BB405B 3V 11.5PF			28381-101V
D2	DI PIN 5082-3379 50V	!		28383-997T
D3	DI PIN 5082-3379 50V	!		28383-997T
D4	DI PIN 5082-3379 50V	!		28383-997T
D5	DI V/CAP BB809 3V 29PF			28381-132G
D6	DI V/CAP BB809 3V 29PF			28381-132G
D7	DI V/CAP BB809 3V 29PF			28381-132G
D8	DI SIL BA482 35V JUNC			28335-675R
D9	DI SIL BA482 35V JUNC			28335-675R
D10	DI SIL BA482 35V JUNC			28335-675R
D11	DI SIL BA482 35V JUNC			28335-675R
D12	DI V/CAP BB405B 3V 11.5PF			28381-101V
D13	DI V/CAP BB405B 3V 11.5PF			28381-101V
D14	DI SIL BA482 35V JUNC			28335-675R
D15	DI SIL BA482 35V JUNC			28335-675R
D16	DI SIL BA482 35V JUNC			28335-675R
D17	DI SIL BA482 35V JUNC			28335-675R
D18	DI SIL BA482 35V JUNC			28335-675R
D20	DI SIL BA482 35V JUNC			28335-675R
D21	DI PIN 5082-3379 50V	!		28383-997T
D22	DI PIN 5082-3379 50V	!		28383-997T
D23	DI SIL BA482 35V JUNC			28335-675R
D24	DI H/CARR HP5082-2811	!		28349-008U
D25	DI SIL BA482 35V JUNC			28335-675R
D26	DI SIL BA482 35V JUNC			28335-675R
D27	DI H/CARR 5082-2080			
D28	DI H/CARR 5082-2080 }	!	Matched set of 4	44529-106X
D29	DI H/CARR 5082-2080			
D30	DI H/CARR 5082-2080			
D31	DI SIL BA482 35V JUNC			28335-675R
D32	DI SIL BA482 35V JUNC			28335-675R
D33	DI H/CARR 5082-2826	!	(Part of matched pair D33/34)	44529-057F
D34	DI V/CAP BB809 3V 29PF			28381-132G
D35	DI V/CAP BB809 3V 29PF			28381-132G
D36	DI V/CAP BB809 3V 29PF			28381-132G
D37	DI V/CAP BB809 3V 29PF			28381-132G
D38	DI PIN 5082-3379 50V	!		28383-997T
D39	DI PIN 5082-3379 50V	!		28383-997T
D40	DI PIN 5082-3379 50V	!		28383-997T
D41	DI PIN 5082-3379 50V	!		28383-997T
D42	DI H/CARR 5082-2826 }	!	Matched pair	44529-057F
D43	DI H/CARR 5082-2826			

Circuit Ref	Description	Part Number
Unit AB1	- RF PROCESSING PCB (Contd.)	
D44	DI H/CARR 5082-2826 ! (Part of matched pair D33/D44)	44529-057F
D45	DI SIL 1N4148 75V JUNC	28336-676J
D46	DI SIL 1N4148 75V JUNC	28336-676J
D47	DI SIL 1N4148 75V JUNC	28336-676J
D48	DI SIL 1N4148 75V JUNC	28336-676J
D49	DI SIL 1N4148 75V JUNC	28336-676J
D50	DI SIL 1N4148 75V JUNC	28336-676J
IC1	MOD HYB OM345 VHF/UHF AMP SIL	28461-351Z
IC2	MOD HYB OM345 VHF/UHF AMP SIL	28461-351Z
IC3	MOD HYB OM345 VHF/UHF AMP SIL	28461-351Z
IC4	ICD INV 74LS04 HEX	28469-171L
IC5	ICD NAND 7438 QUAD 2INP O/C BF	28466-334X
IC6	ICD NAND 74LS26 QUAD 2INP HV	28466-350U
IC7	MOD HYB OM345 VHF/UHF AMP SIL	28461-351Z
IC8	MOD HYB OM345 VHF/UHF AMP SIL	28461-351Z
IC9	MOD HYB OM345 VHF/UHF AMP SIL	28461-351Z
IC10	MOD HYB OM345 VHF/UHF AMP SIL	28461-351Z
IC11	ICD FF D SP9131 DUAL M/SLAVE	28462-112V
IC12	ICA AMP TL072CP DUAL FET I/P	28461-348Z
IC13	MOD HYB OM360 40-860MHZ AMP	28461-366W
IC14	MOD HYB OM360 40-860MHZ AMP	28461-366W
IC15	ICA AMP TL072CP J FET DIL8	28461-348Z
L1	- PRINTED COMPONENT -	
L2	- PRINTED COMPONENT -	
L3	- PRINTED COMPONENT -	
L4	- PRINTED COMPONENT -	
L5	IND CHOKE 2U2 10% MINIATURE	23642-420F
L6	- PRINTED COMPONENT -	
L7	IND CHOKE 2U2 10% MINIATURE	23642-420F
L8	- PRINTED COMPONENT -	
L9	IND CHOKE .47UH 10% LAQ	23642-547Y
L10	- PRINTED COMPONENT -	
L11	- PRINTED COMPONENT -	
L12	- PRINTED COMPONENT -	
L14	- PRINTED COMPONENT -	
L15	- PRINTED COMPONENT -	
L16	IND CHOKE .47UH 10% LAQ	23642-547Y
L17	IND CHOKE 2.2UH 10% LAQ	23642-551N
L18	IND CHOKE .68UH 10% LAQ	23642-548N
L19	IND CHOKE .47UH 10% LAQ	23642-547Y

Circuit Ref	Description	Part Number
Unit AB1	- RF PROCESSING PCB (Contd.)	
L20	- PRINTED COMPONENT -	
L21	- PRINTED COMPONENT -	
L22	- PRINTED COMPONENT -	
L23	- PRINTED COMPONENT -	
L24	IND CHOKE 2.2UH 10% LAQ	23642-551N
L25	IND CHOKE .47UH 10% LAQ	23642-547Y
L26	IND CHOKE 2.2UH 10% MINIATURE	23642-420F
L27	IND CHOKE 2.2UH 10% LAQ	23642-551N
L28	IND CHOKE 2.2UH 10% LAQ	23642-551N
L29	IND CHOKE .1UH 20% LAQ	23642-543Z
L30	IND CHOKE .22UH 10% LAQ	23642-545E
L31	IND CHOKE 2U2 10% MINIATURE	23642-420F
L32	IND CHOKE 10UH 10% LAQ	23642-555G
L33	IND CHOKE 2.2UH 10% MINIATURE	23642-420F
L34	IND CHOKE 2.2UH 10% LAQ	23642-551N
L35	IND CHOKE 2.2UH 10% LAQ	23642-551N
L36	IND CHOKE 2U2 10% MINIATURE	23642-420F
R1	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R2	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R3	RES MF 100R 1/4W 2% 100PPM	24773-249J
R4	RES MF 68K 1/4W 2% 100PPM	24773-317N
R5	RES MF 100R 1/4W 2% 100PPM	24773-249J
R6	RES MF 47R 1/4W 2% 100PPM	24773-241A
R7	RES MF 47R 1/4W 2% 100PPM	24773-241A
R8	RES MF 10K 1/4W 2% 100PPM	24773-297M
R9	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R10	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R11	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R12	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R13	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R14	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R15	RES MF 22R 1/4W 2% 100PPM	24773-233M
R16	RES CC 10R 1/8W 5%	24331-974U
R17	RES MF 10K 1/4W 2% 100PPM	24773-297M
R18	RES MG 4M7 1/4W 5%	24321-881F
R19	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R20	RES MF 220R 1/4W 2% 100PPM	24773-257W
R21	RES MF 47K 1/4W 2% 100PPM	24773-313H
R22	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R23	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R24	RES MF 100R 1/4W 2% 100PPM	24773-249J
R25	RES MF 2K2 1/4W 2% 100PPM	24773-281Y

Circuit Ref	Description	Part Number
Unit AB1	- RF PROCESSING PCB (Contd.)	
R26	RES MF 10K 1/4W 2% 100PPM	24773-297M
R27	RES CC 43R 1/8W 5%	24331-995C
R28	RES MF 470R 1/4W 2% 100PPM	24773-265M
R29	RES MF 100R 1/4W 2% 100PPM	24773-249J
R30	RES MF 100R 1/4W 2% 100PPM	24773-249J
R31	RES MF 100R 1/4W 2% 100PPM	24773-249J
R32	RES CC 22R 1/8W 5%	24331-988T
R33	RES CC 22R 1/8W 5%	24331-988T
R34	RES CC 10R 1/8W 5%	24331-974U
R35	RES MF 100R 1/4W 2% 100PPM	24773-249J
R36	RES MF 10K 1/4W 2% 100PPM	24773-297M
R37	RES CC 56R 1/8W 5%	24331-944N
R38	RES MF 470R 1/4W 2% 100PPM	24773-265M
R39	RES MF 100R 1/4W 2% 100PPM	24773-249J
R40	RES MF 100R 1/4W 2% 100PPM	24773-249J
R41	RES MF 100R 1/4W 2% 100PPM	24773-249J
R42	RES CC 22R 1/8W 5%	24331-988T
R43	RES CC 22R 1/8W 5%	24331-988T
R44	RES CC 10R 1/8W 5%	24331-974U
R45	RES MF 100R 1/4W 2% 100PPM	24773-249J
R46	RES MF 100R 1/4W 2% 100PPM	24773-249J
R47	RES MF 100R 1/4W 2% 100PPM	24773-249J
R48	RES MF 100R 1/4W 2% 100PPM	24773-249J
R49	RES MF 100R 1/4W 2% 100PPM	24773-249J
R50	RES MF 30R 1/4W 2% 100PPM	24773-236B
R51	RES MF 10K 1/4W 2% 100PPM	24773-297M
R52	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R53	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R54	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R55	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R56	RES MF 100K 1/4W 2% 100PPM	24773-321L
R57	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R58	RES MF 330R 1/4W 2% 100PPM	24773-261D
R59	RES MF 270R 1/4W 2% 100PPM	24773-259T
R60	RES MF 330R 1/4W 2% 100PPM	24773-261D
R61	RES MF 270R 1/4W 2% 100PPM	24773-259T
R62	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R63	RES MF 100K 1/4W 2% 100PPM	24773-321L
R64	RES MF 100K 1/4W 2% 100PPM	24773-321L
R65	RES CC 10R 1/8W 5%	24331-974U

Circuit Ref	Description	Part Number
Unit AB1	- RF PROCESSING PCB	(Contd.)
R66	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R67	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R68	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R69	RES MF 62R 1/4W 2% 100PPM	24773-244E
R70	RES CC 51R 1/8W 5%	24331-989P
R71	RES MF 330R 1/4W 2% 100PPM	24773-261D
R72	RES CC 18R 1/8W 5%	24331-943Y
R73	RES MF 330R 1/4W 2% 100PPM	24773-261D
R74	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R75	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R76	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R77	RES MF 2K2 1/4W 2% 100PPM	24773-284Y
R78	RES MF 270R 1/4W 2% 100PPM	24773-259T
R79	RES MF 270R 1/4W 2% 100PPM	24773-259T
R80	RES CC 47R 1/8W 5%	24331-975Y
R81	RES MF 47K 1/4W 2% 100PPM	24773-313H
R82	RES MF 220K 1/4W 2% 100PPM	24773-329T
R83	RES CC 51R 1/8W 5%	24331-989P
R84	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R85	RES MF 15K 1/4W 2% 100PPM	24773-301P
R86	RES MF 470R 1/4W 2% 100PPM	24773-265M
R87	RES MF 33R 1/4W 2% 100PPM	24773-237K
R88	RES MF 10R 1/4W 2% 100PPM	24773-225W
R89	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R90	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R91	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R92	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R93	RES MF 220R 1/4W 2% 100PPM	24773-257W
R94	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R95	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R96	RES MO 150R 1/2W 2% 250PPM	24573-053K
R97	RES CC 47K 1/8W 5%	24331-982F
R98	RES CC 100R 1/8W 5%	24331-997B
R99	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R100	RES MF 100K 1/4W 2% 100PPM	24773-321L
R101	RV CERM 100K LIN .5W 10% HORZ	25711-644W
R102	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R103	RES MG 10M 1/4W 5%	24321-885W
R104	RES MF 470K 1/4W 2% 100PPM	24773-337R
R105	RES MF 470K 1/4W 2% 100PPM	24773-337R

Circuit Ref	Description	Part Number
Unit AB1	- RF PROCESSING PCB (Contd.)	
R106	RES MG 10M 1/4W 5%	24321-885W
R107	RES CC 47K 1/8W 5%	24331-982F
R108	RES MF 100K 1/4W 2% 100PPM	24773-321L
R109	RES MF 220R 1/4W 2% 100PPM	24773-257W
R110	RES MF 10K 1/4W 2% 100PPM	24773-297M
R111	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R112	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R113	RES MF 220R 1/4W 2% 100PPM	24773-257W
R114	RES MF 24K 1/4W 2% 100PPM	24773-306B
R116	RES MF 470K 1/4W 2% 100PPM	24773-337R
R118	RES MF 470K 1/4W 2% 100PPM	24773-337R
R119	RES MF 100R 1/4W 2% 100PPM	24773-249J
R120	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R121	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R122	RES MF 50R0 1/4W 1% 100PPM NI	24762-558R
R123	RES CC 47R 1/8W 5%	24331-975Y
R124	RES MF 5K1 1/10W 1% 100PPM	24421-598W
R125	RES CC 100R 1/8W 5%	24331-997B
R126	RES MF 3K0 1/4W 2% 100PPM	24773-284J
R127	RES MF 12K 1/4W 2% 100PPM	24773-299R
RLA	RELAY MAG 2CO 5V 100R	23486-146C
TR1	TR NJF J310 25V - 24MA	28459-028E
TR2	DI CUR REG J510 3.6MA TO92	28383-984Y
TR3	TR PSI 2N4959 25V 1.4G - LN AMP	28433-836K
TR4	TR PSI 2N4959 25V 1.4G - LN AMP	28433-836K
TR5	TR PSI BC308B 20V 130M - GEN	28433-455R
TR6	TR NSI BC208B 20V 150M - GEN	28452-781A
TR7	TR NSI BFR91A 12V 5G - AMP	28451-694H
TR8	TR PSI BC308B 20V 130M - GEN	28433-455R
TR9	TR NSI BC208B 20V 150M - GEN	28452-781A
TR10	TR NSI BFR91A 12V 5G - AMP	28451-694H
TR11	TR NSI BFR91A 12V 5G - AMP	28451-694H
TR12	TR NSI 2N5109 40V 200M - AMP	28454-797G
TR13	TR PSI BC308B 20V 130M - GEN	28433-455R
T1	TRANSFORMER ASSY (3.5 TURNS)	43590-140U
T4	TRANSFORMER ASSY (3.5 TURNS)	43590-140U
T5	TRANSFORMER ASSY (1.5 TURNS)	43590-143L
T6	- PRINTED COMPONENT -	
X1	MOD RF TFM2 DOUBLE BAL MIXER	28531-003Z

Circuit Ref	Description	Part Number
Unit AC0	- ATTENUATOR	
15. When ordering, prefix circuit reference with AC0		
	Complete unit	44429-029N
MP1	ATTENUATOR BODY	34901-001C
MP2	ATTENUATOR LID	34901-002R
Unit AC1	- ATTENUATOR PCB	
16. When ordering, prefix circuit reference with AC1		
	Complete unit	44828-789N
C1	CAP CER 15P 63V 5% PLATE	26343-467U
C2	CAP CER 1N0 63V 10% PLATE	26383-585M
C3	CAP CER 15P 63V 5% PLATE	26343-467U
C4	CAP CER 1N0 63V 10% PLATE	26383-585M
C5	CAP CER 15P 63V 5% PLATE	26343-467U
C6	CAP CER 1N0 63V 10% PLATE	26383-585M
C7	CAP CER 15P 63V 5% PLATE	26343-467U
C8	CAP CER 1N0 63V 10% PLATE	26383-585M
C9	CAP CER 15P 63V 5% PLATE	26343-467U
C10	CAP CER 1N0 63V 10% PLATE	26383-585M
C11	CAP CER 15P 63V 5% PLATE	26343-467U
C12	CAP CER 1N0 63V 10% PLATE	26383-585M
C13	CAP CER 15P 63V 5% PLATE	26343-467U
C14	CAP CER 1N0 63V 10% PLATE	26383-585M
C15	CAP CER 15P 63V 5% PLATE	26343-467U
C16	CAP CER 1N0 63V 10% PLATE	26383-585M
D1	DI H/CARR HP5082-2811	28349-008U
D2	DI H/CARR HP5082-2811	28349-008U
L1	IND CHOKE 2.2UH 10% LAQ	23642-551N
L2	IND CHOKE 2.2UH 10% LAQ	23642-551N
L3	IND CHOKE 2.2UH 10% LAQ	23642-551N
L4	IND CHOKE 2.2UH 10% LAQ	23642-551N
L5	IND CHOKE 2.2UH 10% LAQ	23642-551N
L6	IND CHOKE 2.2UH 10% LAQ	23642-551N
L7	IND CHOKE 2.2UH 10% LAQ	23642-551N
L8	IND CHOKE 2.2UH 10% LAQ	23642-551N
L9	IND CHOKE 2.2UH 10% LAQ	23642-551N
PLN	CON PCB MALE 36 FXD STRAIGHT	23435-121J

Circuit Ref	Description	Part Number
Unit AC1	- ATTENUATOR PCB (Contd.)	
R1	RES MF 53R3 1/4W 1% 100PPM NI	24762-557C
R2	RES MF 790R 1/4W 1% 100PPM NI	24762-646F
R3	RES MF 53R3 1/4W 1% 100PPM NI	24762-557C
R4	RES MF 61R1 1/4W 1% 100PPM NI	24762-571U
R5	RES MF 247R 1/4W 1% 100PPM NI	24762-631R
R6	RES MF 61R1 1/4W 1% 100PPM NI	24762-571U
R7	RES MF 53R3 1/4W 1% 100PPM NI	24762-557C
R8	RES MF 790R 1/4W 1% 100PPM NI	24762-646F
R9	RES MF 53R3 1/4W 1% 100PPM NI	24762-557C
R10	RES MF 96R3 1/4W 1% 100PPM NI	24762-582S
R11	RES MF 71R2 1/4W 1% 100PPM NI	24762-572Y
R12	RES MF 96R3 1/4W 1% 100PPM NI	24762-582S
R13	RES MF 53R3 1/4W 1% 100PPM NI	24762-557C
R14	RES MF 790R 1/4W 1% 100PPM NI	24762-646F
R15	RES MF 53R3 1/4W 1% 100PPM NI	24762-557C
R16	RES CC 1KO 1/8W 5%	24331-967A
R17	RES CC 100R 1/8W 5%	24331-997B
RLA	RELAY MAG 2CO 5V 100R TO5	23486-156E
RLB	RELAY MAG 2CO 5V 100R TO5	23486-156E
RLC	RELAY MAG 2CO 5V 100R TO5	23486-156E
RLD	RELAY MAG 2CO 5V 100R TO5	23486-156E
RLE	RELAY MAG 2CO 5V 100R TO5	23486-156E
RLF	RELAY MAG 2CO 5V 100R TO5	23486-156E
Unit AD0	- GPIB MODULE	
17. When ordering, prefix circuit reference with AD0		
	Complete unit	54433-003N
MP1	SHROUD MOUNTING	35904-293P
MP2	SPACER SPECIAL ST/CD STUDMOUNT	33900-539L
Unit AD1	- GPIB PCB	
18. When ordering, prefix circuit reference with AD1		
	Complete unit	44828-785H
C1	CAP PETP 470N 63V 10% RAD MIN	26582-427L
C2	CAP PETP 470N 63V 10% RAD MIN	26582-427L
C3	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C4	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C5	CAP CER 10N 50V 20% X7R MON AX	26346-120Y

Circuit Ref	Description	Part Number
Unit A01	- GPIB PCB (Contd.)	
C6	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C7	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C8	CAP CER 2N2 63V 10% PLATE	26383-587R
IC1	ICD INV 74LS14 HEX SCHM	28469-176S
IC2	ICD MP SUP 8291A GPIB TALK/LIS !	28467-014C
IC3	ICD BUFF 3448 QUAD GPIBTXRX 3S	28469-190R
IC4	ICD BUFF 3448 QUAD GPIBTXRX 3S	28469-190R
IC5	ICD BUFF 3448 QUAD GPIBTXRX 3S	28469-190R
IC6	ICD BUFF 3448 QUAD GPIBTXRX 3S	28469-190R
L1	IND CHOKE 100UH 10% LAQ	23642-561W
R1	RES MF 330R 1/4W 2% 100PPM	24773-261D

MECHANICAL COMPONENTS

19. Order without prefix.

Fig. 1 Item	Description	Part Number
1	Button outer cover	35903-668Y
2	Front panel switch caps (see keyboard, Unit A1 for individual part numbers)	
3	Front panel, screen printed	35890-084K
4	Frame casting; front, painted	35890-084K
5	Plug	37590-293K
6	Foot	37590-224R
7	Top cover - stone grey	35904-009F
8	Rear frame casting	35890-101L
9	Rear foot	37590-840M
10	Side rail	34900-812Z
11	Selector plate	35902-441Z
12	GPIB blanking plate	35904-290W
13	Cap	37590-219M
14	Boss	37590-220P
15	Handle assembly	41700-239W

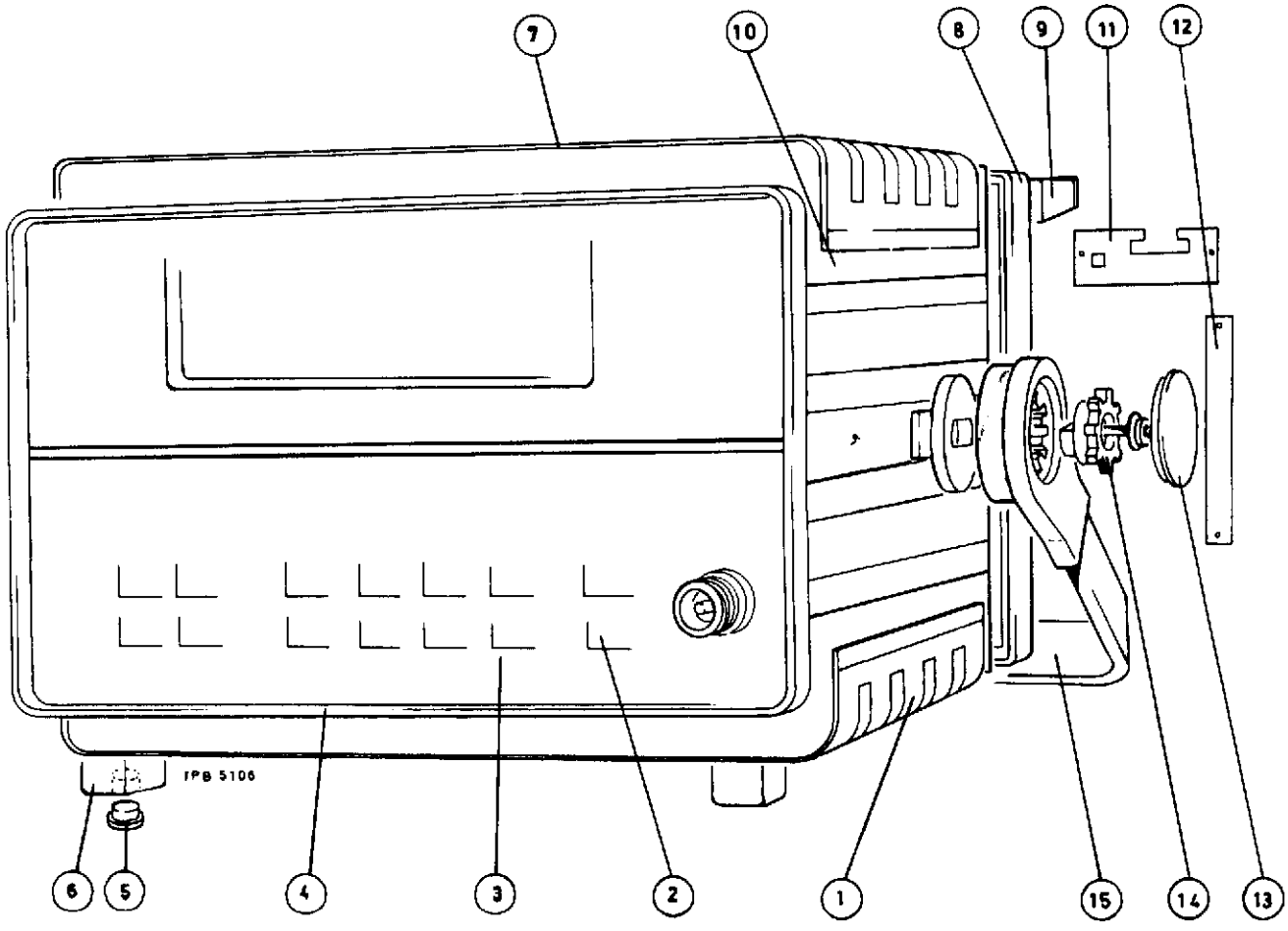


Fig. 1 Miscellaneous mechanical components

Chapter 7

SERVICING DIAGRAMS

CONTENTS

CIRCUIT NOTES

Component values

1. Resistors : Code letter R = ohms, k = kilohms (10^3), M = megohms (10^6).

Capacitors : Code letter m = millifarads (10^{-3}) μ = microfarads (10^{-6}), n = nanofarads (10^9), P = picofarads (10^{-12}).

Inductors : Code letter H = henrys, m = millihenrys (10^{-3}), μ = microhenrys (10^{-6}), n = nanohenrys (10^{-9}).

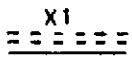
SIC : Value selected during test, nominal value shown.

2. Components are marked normally with two, three for four figures according to the accuracy limit ±10%, ±1% or ±0.1%. The code letter used indicates the multiplier and replaces the decimal point. Because a marked 4m7 could be interpreted as milliohms, millifarads or millihenrys all values are placed near to their related circuit symbol.

Symbols

3. Symbols are based on the provisions of BS 3939 with the following additions:-


edge connector

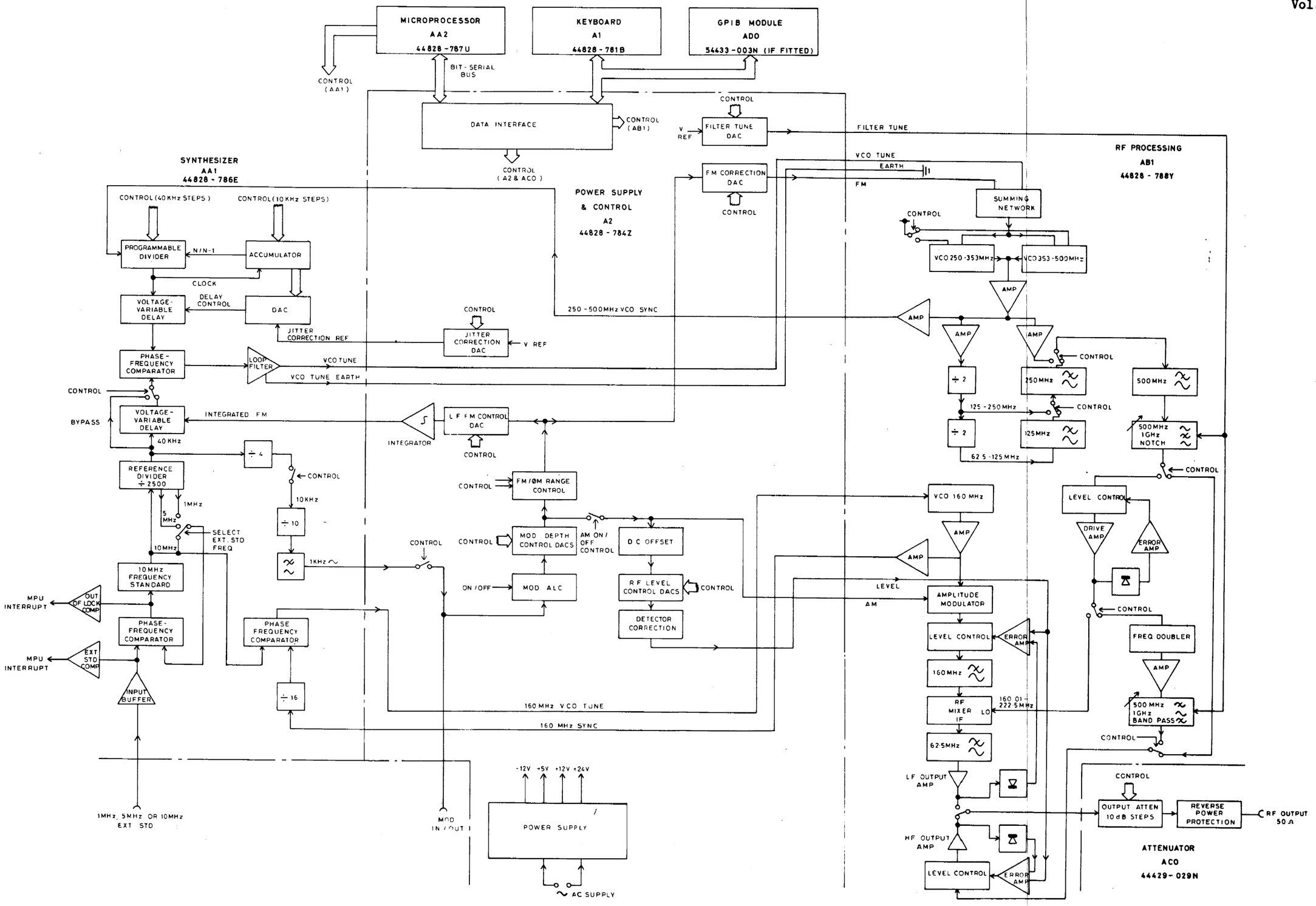


ferrite bead


warning, see page (iv), notes and cautions

unit identification number

P printed component



2022 Frequency synthesis and signal processing simplified block diagram

Fig. 1

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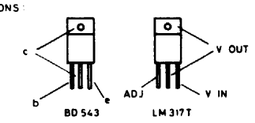
NOTES

1 MATING PLUGS AND SOCKETS HAVE SAME IDENTITY. FOR EXAMPLE SKF CONNECTS TO PLF. CONNECTOR NUMBERS CORRESPOND IF SOCKETS AT BOTH ENDS OF A CONNECTOR ASSEMBLY HAVE SAME IDENTITY (IE PIN 1 CONNECTS TO PIN 1, PIN 2 TO PIN 2 ETC.)

2 WIRE TYPES: 6^a 15410-227T, 6^b 15410-222G, 6^c 15420-276U, 6^d 15410-187W, 6^e 15410-202C, 6^f M15410-181, 6^g 15110-222S.

3 VIEWED FROM FRONT OF INSTRUMENT SWITCH SB IS TO THE RIGHT OF SC. CONTACT POSITIONS MARKED ALSO REFER TO VIEW FROM FRONT OF INSTRUMENT. SB IS DRAWN FOR 210-240V SUPPLY (ALTERNATIVE POSITION IS FOR 105-120V). SC IS DRAWN FOR 115/120V OR 230/240V (ALTERNATIVE POSITION IS FOR 105/110V OR 210/220V).

4 LEAD CONFIGURATIONS:



5 ≡≡≡ INDICATES FERRITE BEAD.

6. THE NEGATIVE TERMINAL OF FAN IS CONNECTED TO POSITIVE SUPPLY SO THAT AIR FLOWS OUT OF REAR PANEL.

Basic module interconnections, A0

Fig. 2

Sep. 86 (Am. 2)

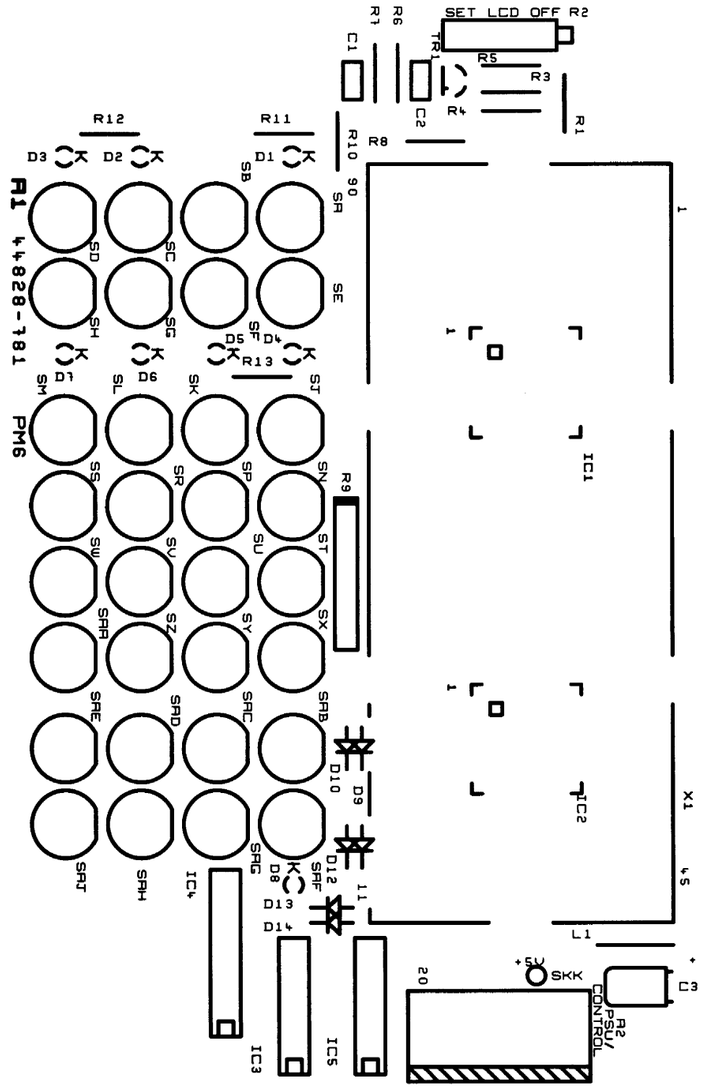


Fig. 3a
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Keyboard component layout, A1

Fig. 3a

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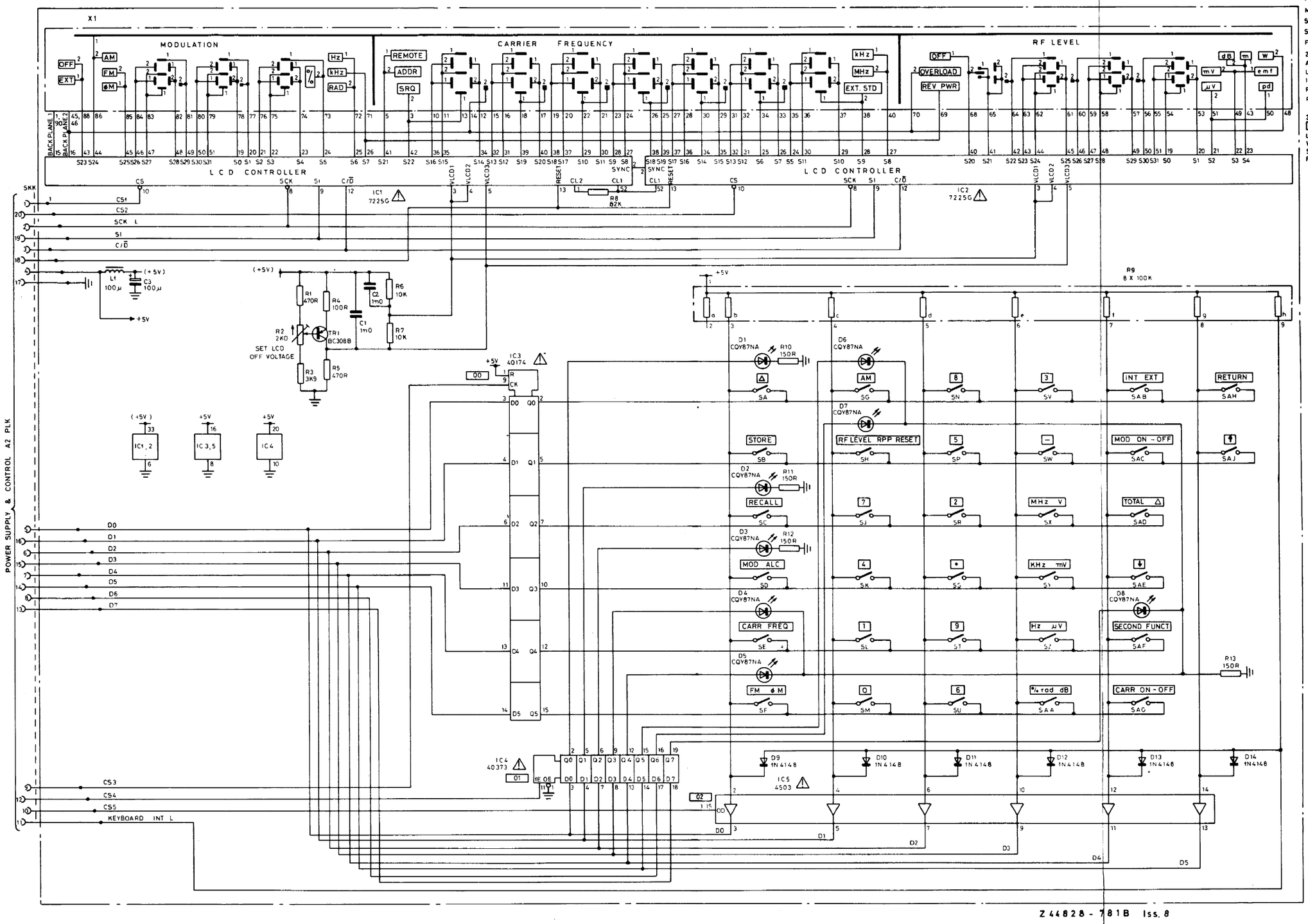
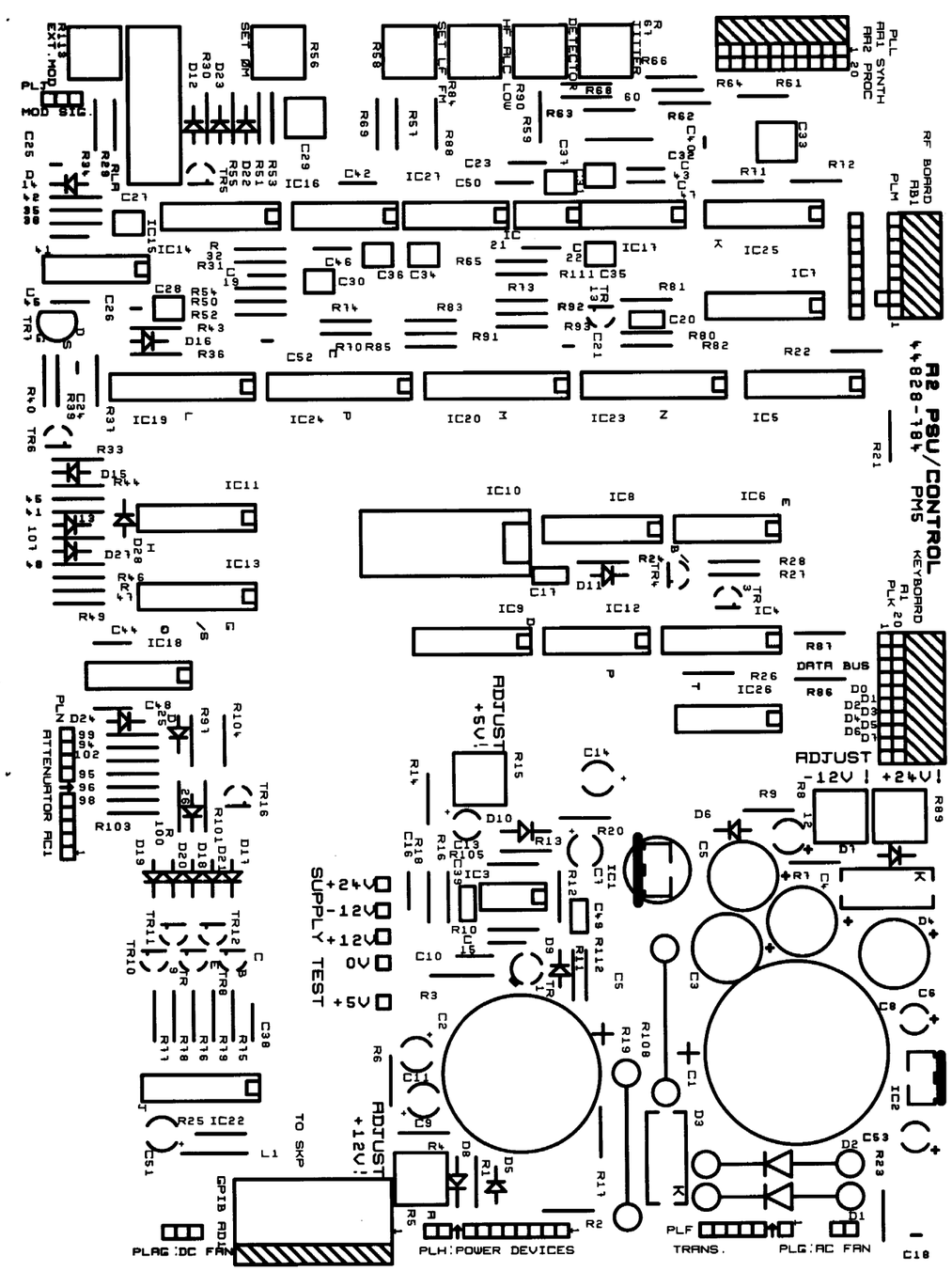
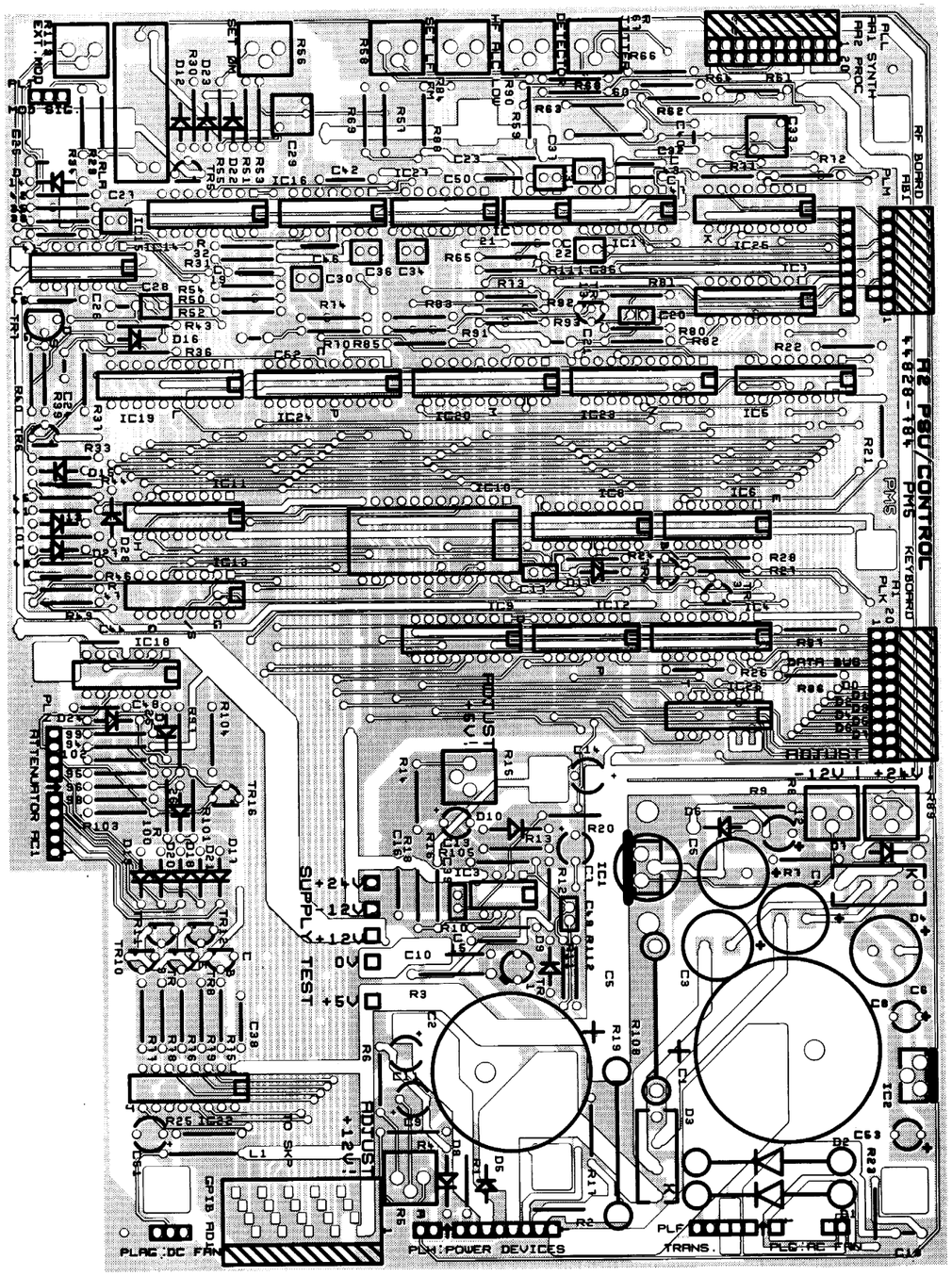


Display and keyboard, A1

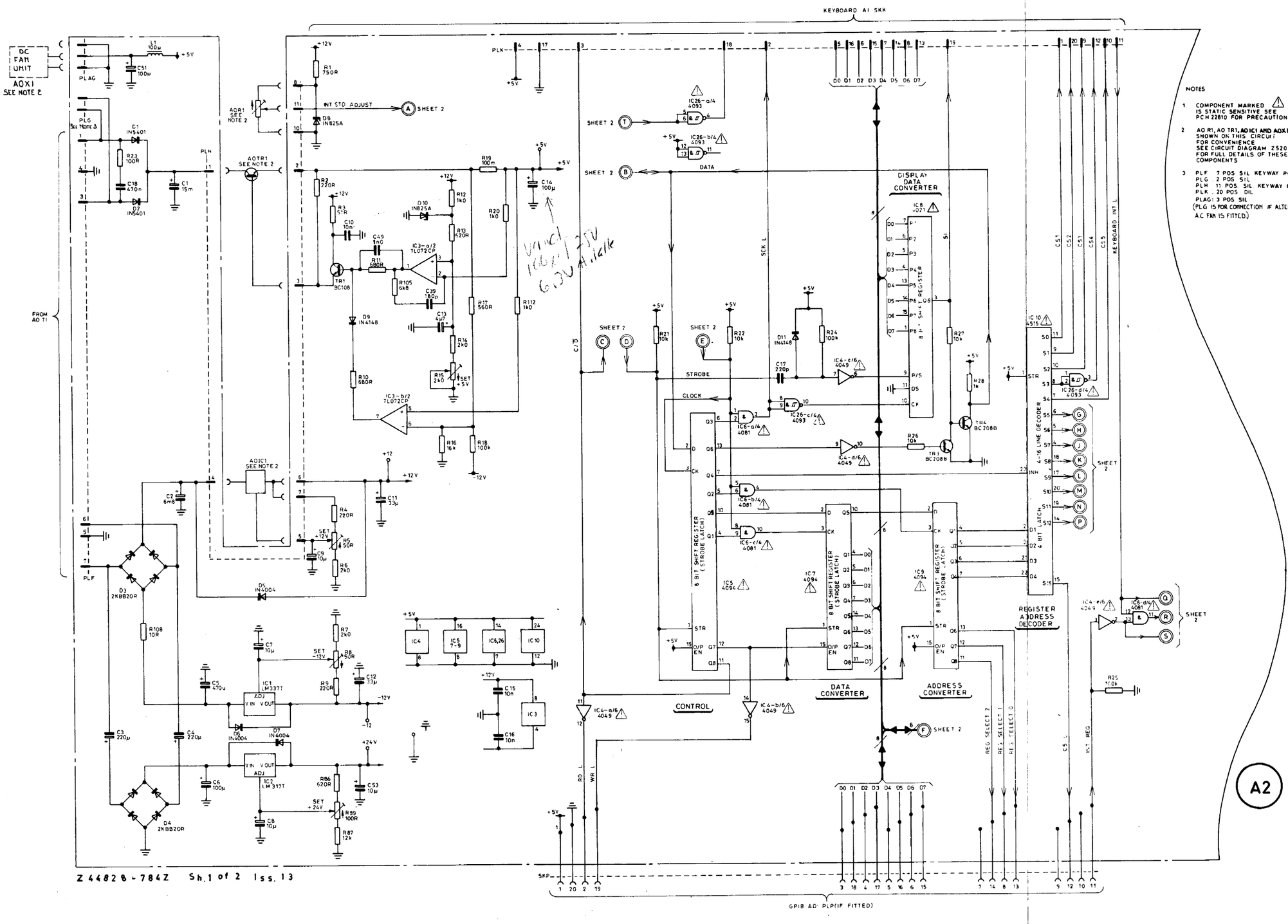
Fig. 3

Apr. 85 (Am.1)

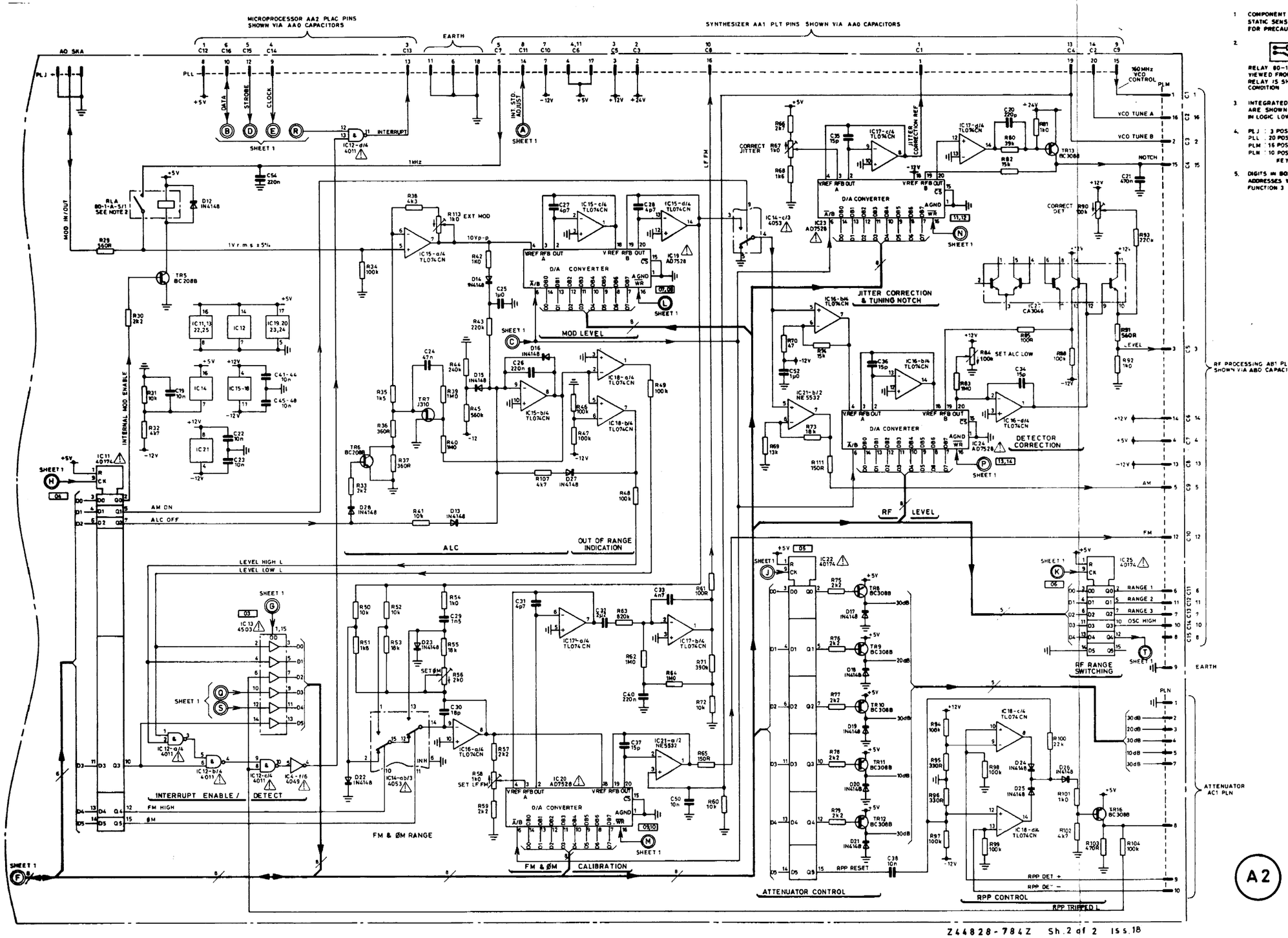




Power supply & control, component layout, A2



Power supply & control (Sheet 1), A2



1 COMPONENT MARKED ⚠ IS STATIC SENSITIVE SEE PCH 22810 FOR PRECAUTIONS.

2

RELAY 80-1-A-5/1 CONNECTIONS VIEWED FROM PIN SIDE RELAY IS SHOWN IN NON-ENERGISED CONDITION

3 INTEGRATED CIRCUIT SWITCHES ARE SHOWN FOR CONTROLS IN LOGIC LOW CONDITION

4. PLJ : 3 POS SIL.
PLL : 20 POS DIL
PLM : 16 POS DIL.
PLN : 10 POS SIL.
KEYWAY POS 5

5. DIGITS IN BORES ▭ SHOW LATCH ADDRESSES WHEN USING SECOND FUNCTION 3

Z44828-784Z Sh.2 of 2 Iss.18

Power supply & control (Sheet 2), A2

Fig. 5

Sep. 86 (Am. 2)

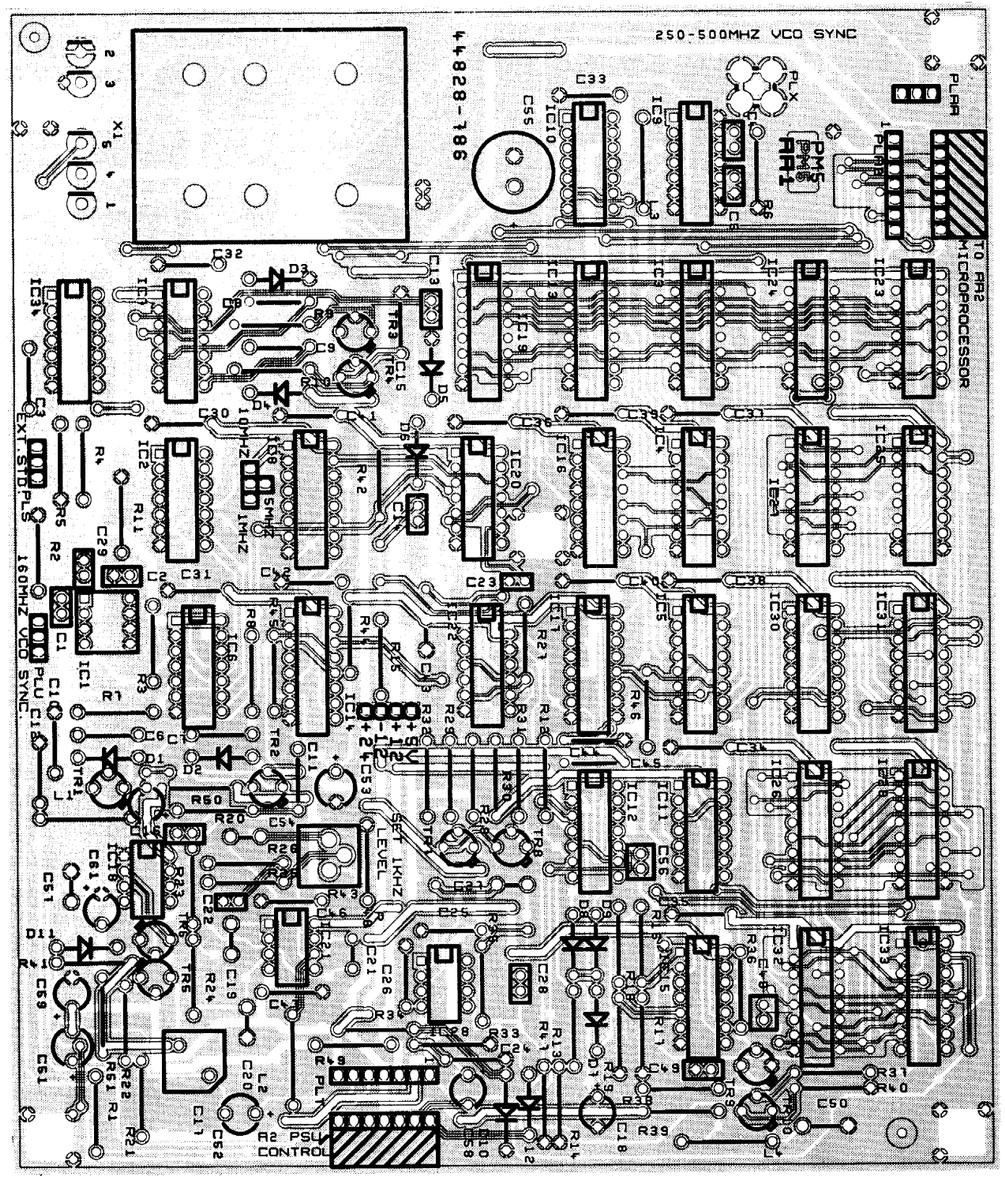


Fig. 6a
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Synthesizer, component layout, AA1

Fig. 6a

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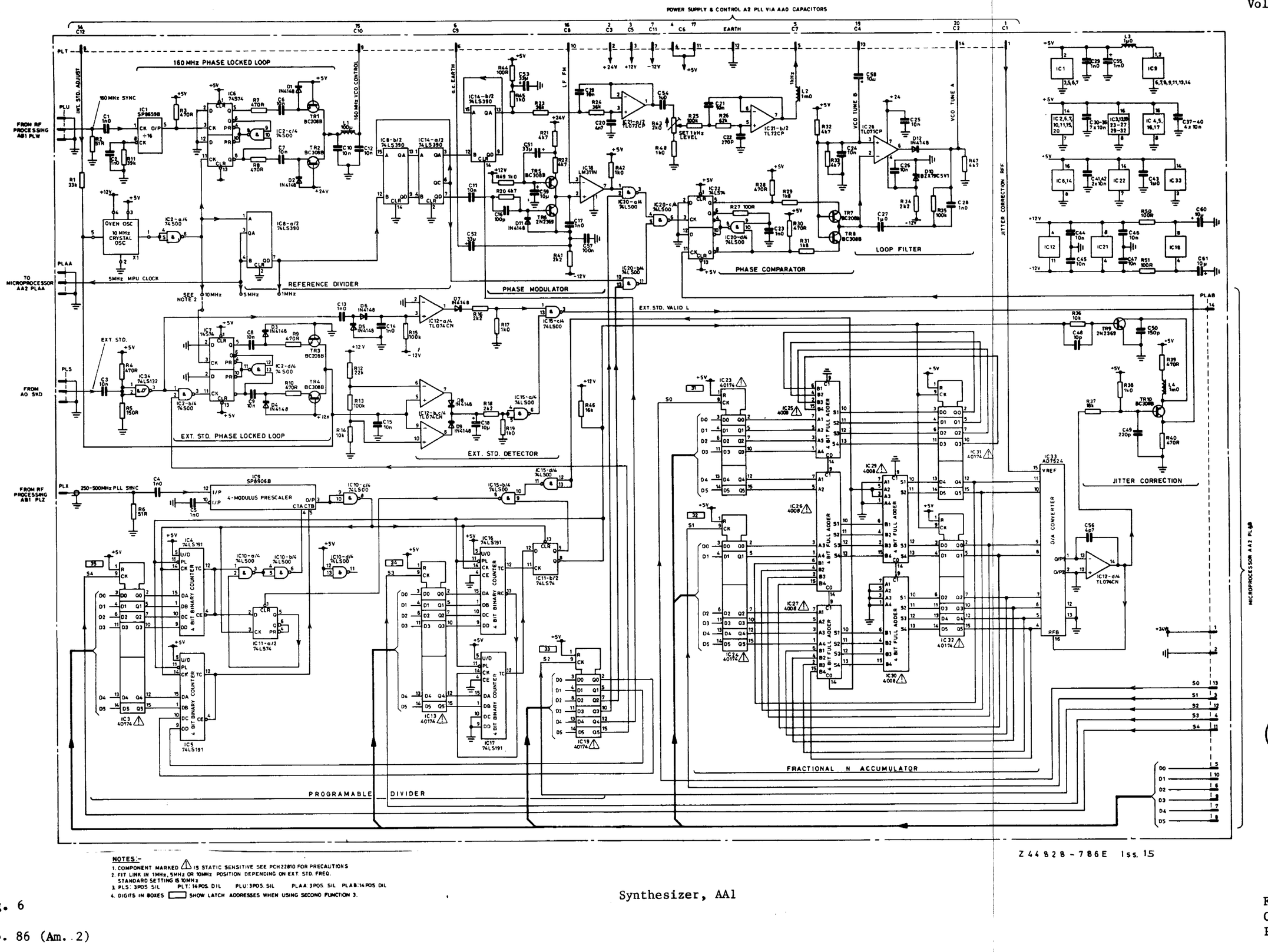

NOTES:-
1. COMPONENT MARKED ⚠ IS STATIC SENSITIVE SEE PCH22810 FOR PRECAUTIONS
2. FIT LINK IN 1MHz, 5MHz OR 10MHz POSITION DEPENDING ON EXT. STD. FREQ. STANDARD SETTING IS 10MHz
3. PLS: 3POS SIL PLT: 14POS DIL PLU: 3POS SIL PLAA 3POS SIL PLAB:14POS DIL
4. DIGITS IN BOXES ☐ SHOW LATCH ADDRESSES WHEN USING SECOND FUNCTION 3.

Fig. 6

Synthesizer, AA1

Sep. 86 (Am. 2)

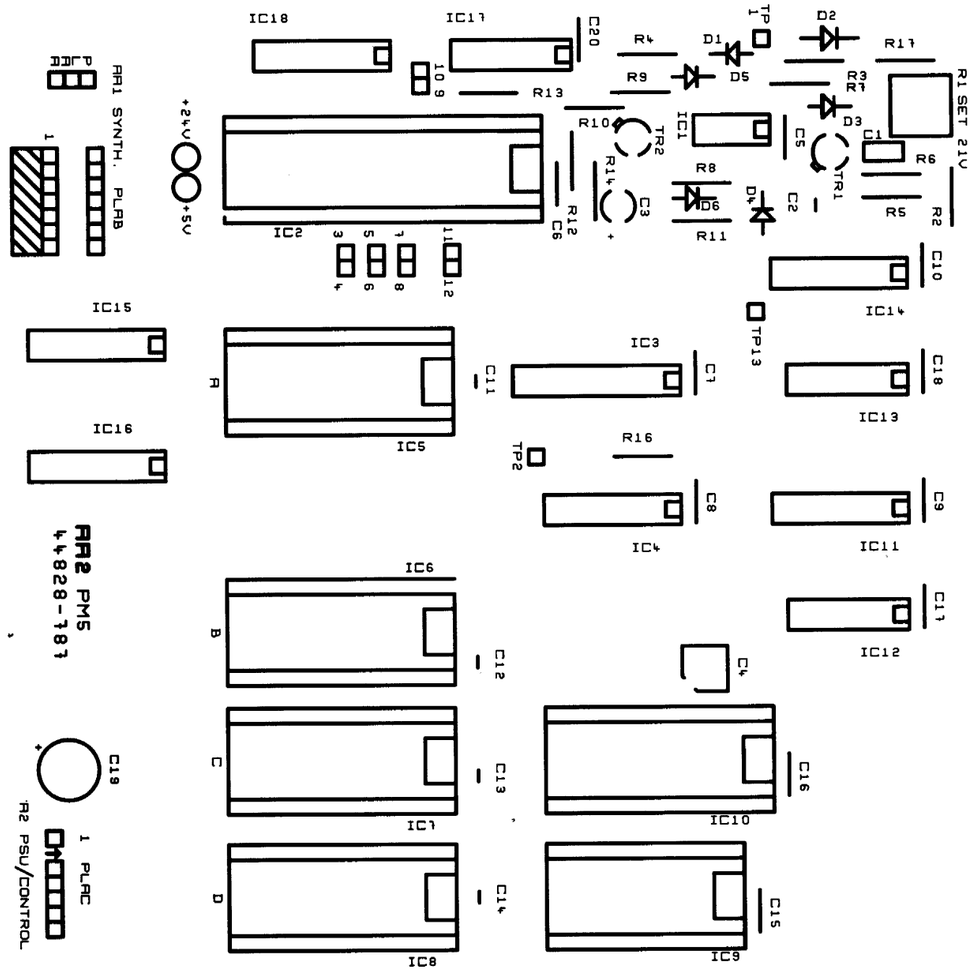

Fig. 7a
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Microprocessor, component layout, (AA2)

Fig. 7a

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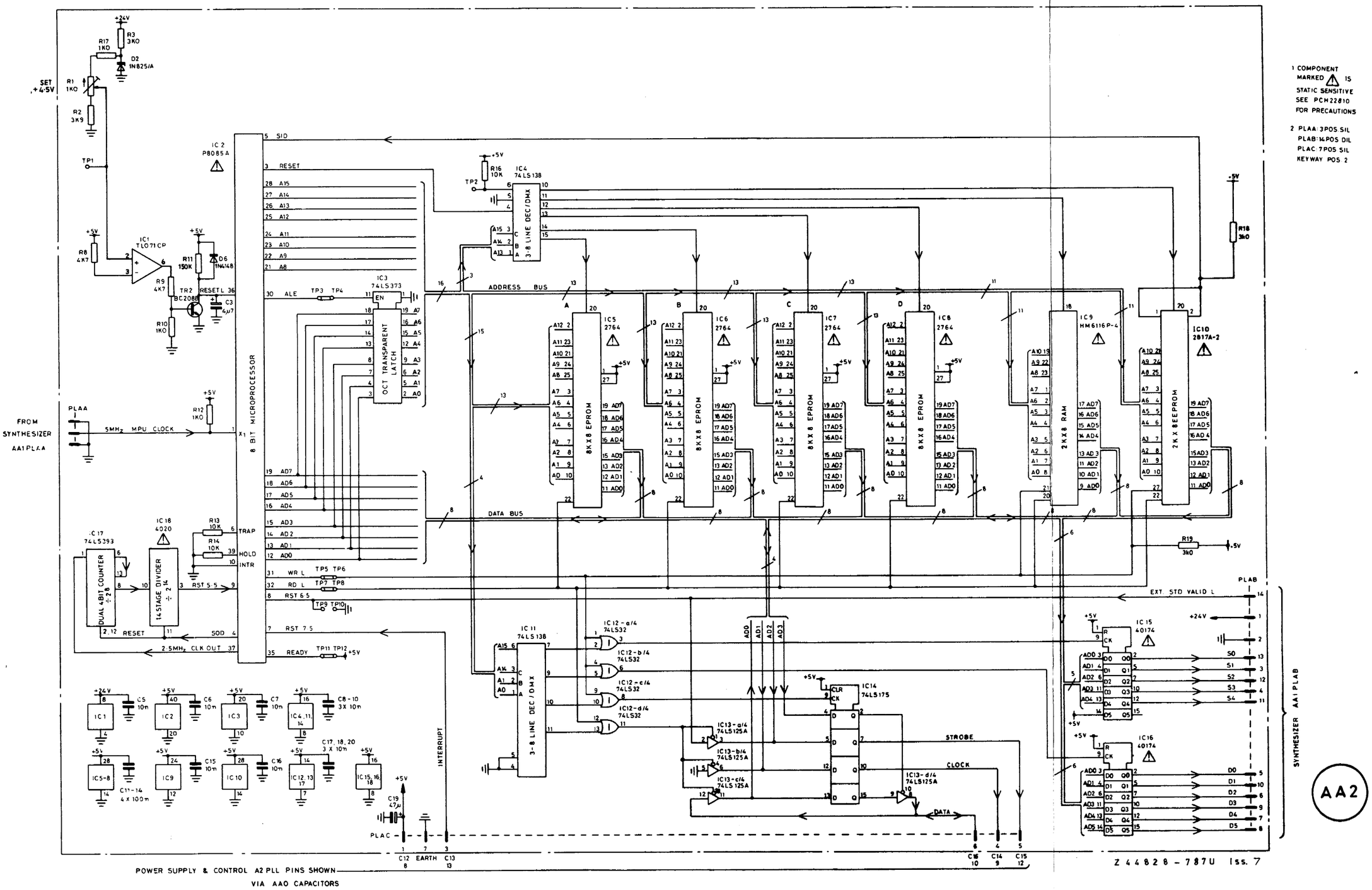

Microprocessor, AA2

Fig. 7

Sep. 86 (Am. 2)

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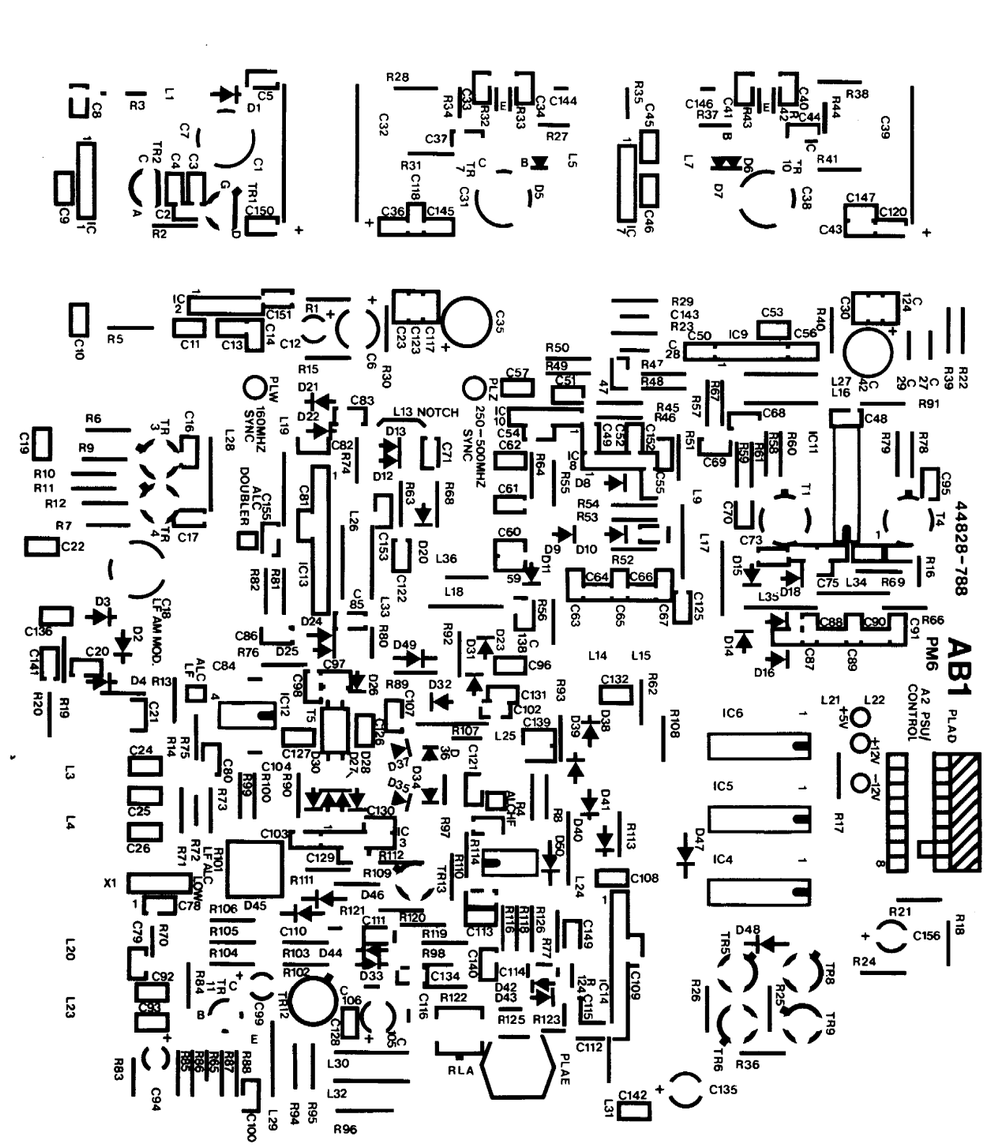

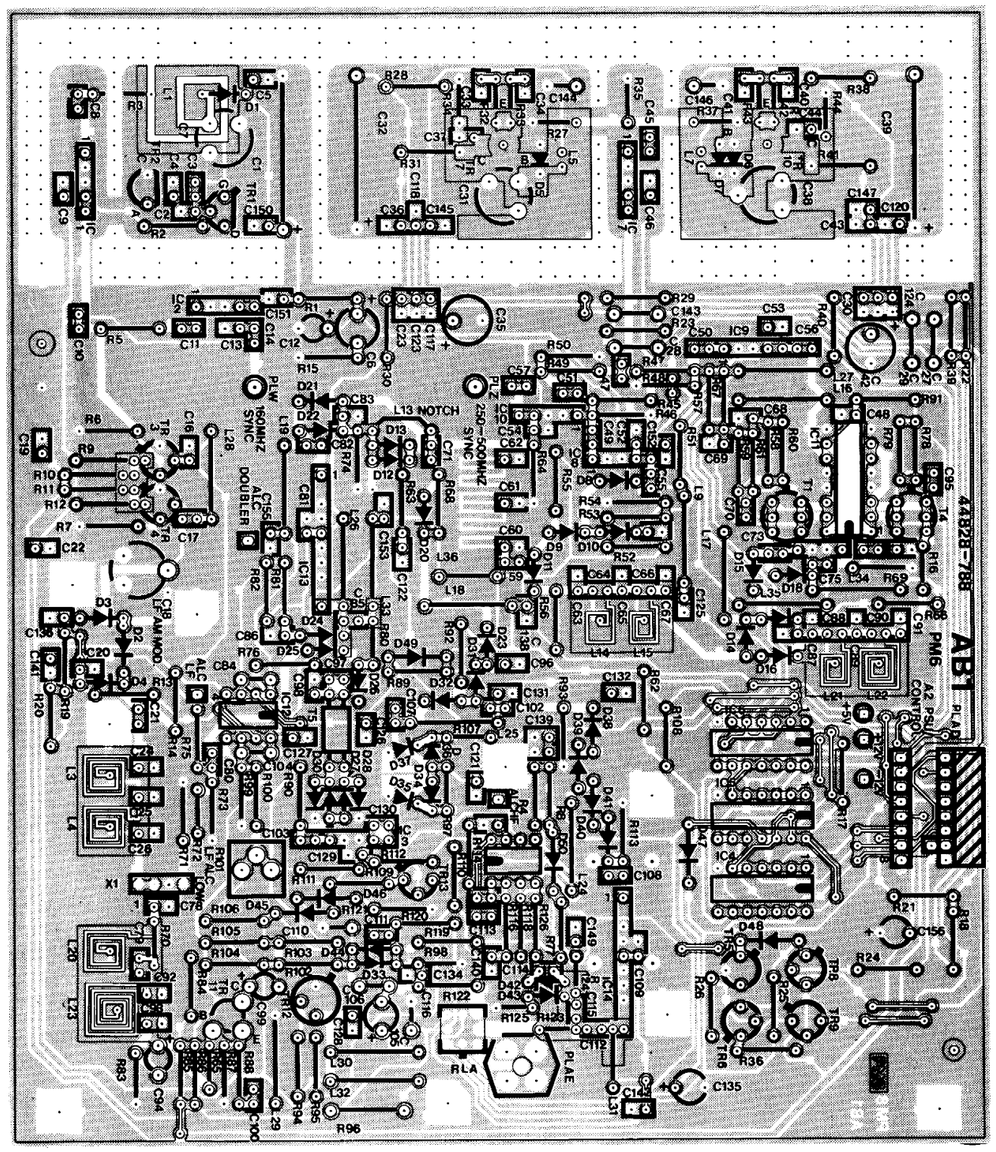

RF processing, component layout, AB1

Fig. 8a
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Fig. 8a

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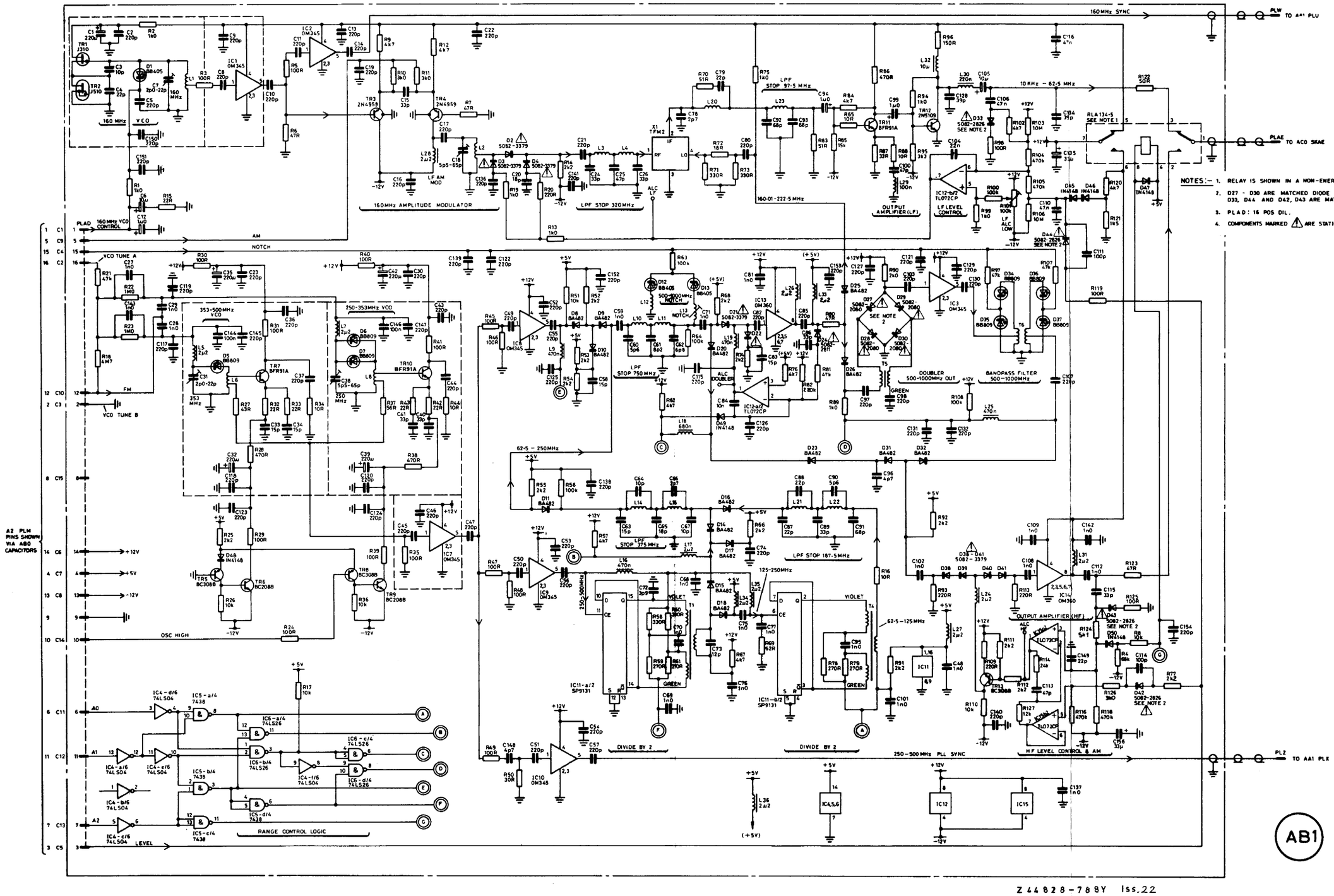

NOTES:–

1. RELAY IS SHOWN IN A NON-ENERGIZED CONDITION.
2. D27 – D30 ARE MATCHED DIODE QUAD. D33, D44 AND D42, D43 ARE MATCHED DIODE PAIRS.
3. PLAD: 16 POS DIL.
4. COMPONENTS MARKED ⚠ ARE STATIC SENSITIVE

RF processing, AB1

Fig. 8

Sep. 86 (Am. 2)

Fig. 8
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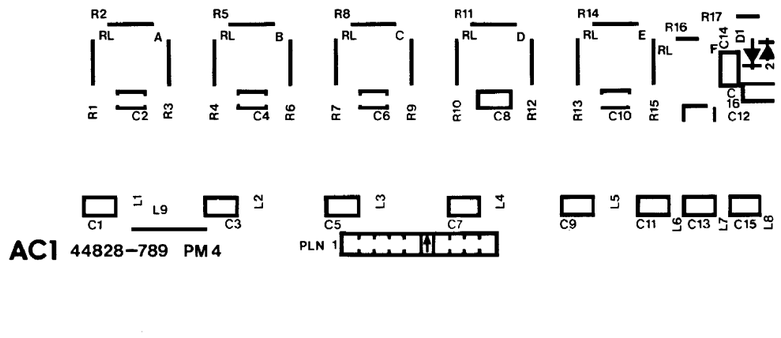
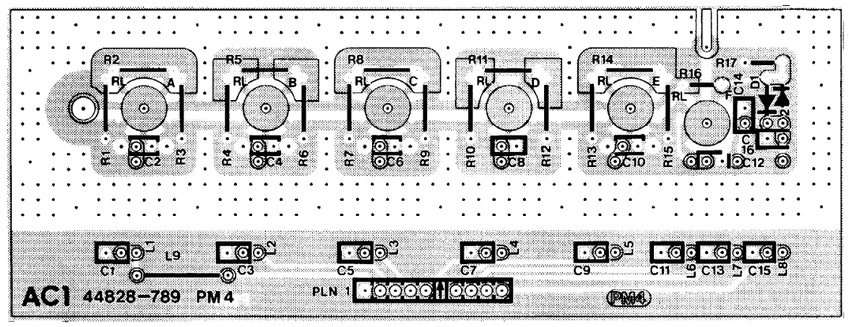
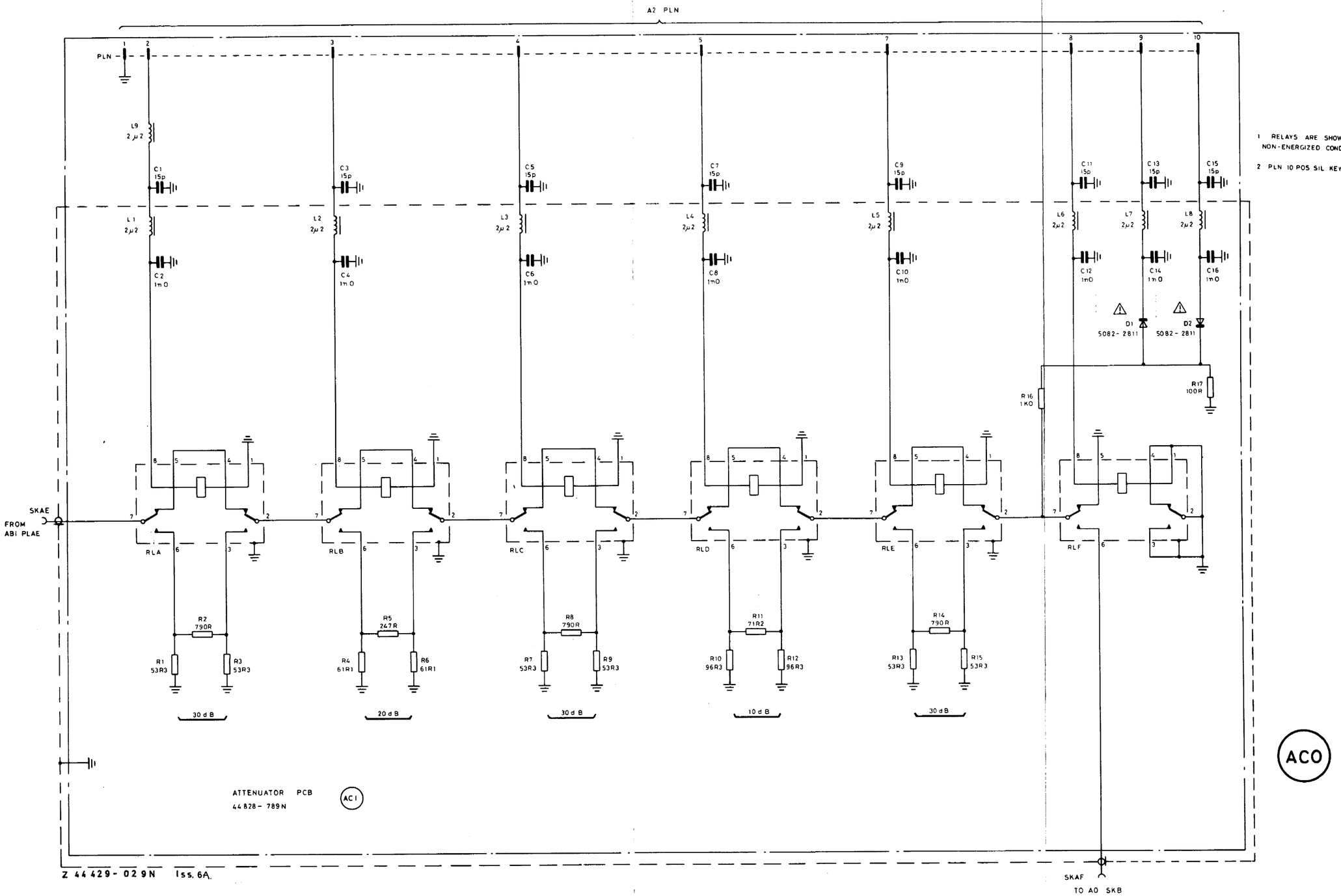




Attenuator, component layout, AC1



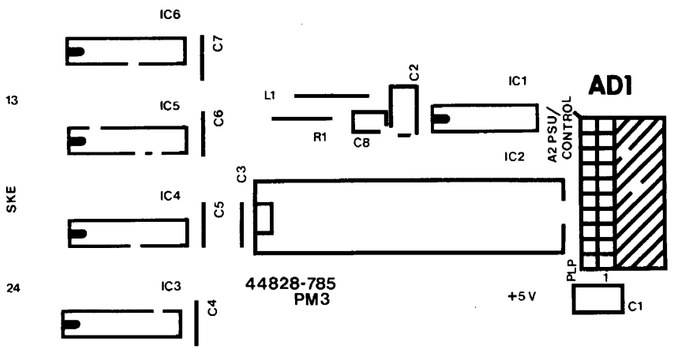
1 RELAYS ARE SHOWN IN NON-ENERGIZED CONDITION

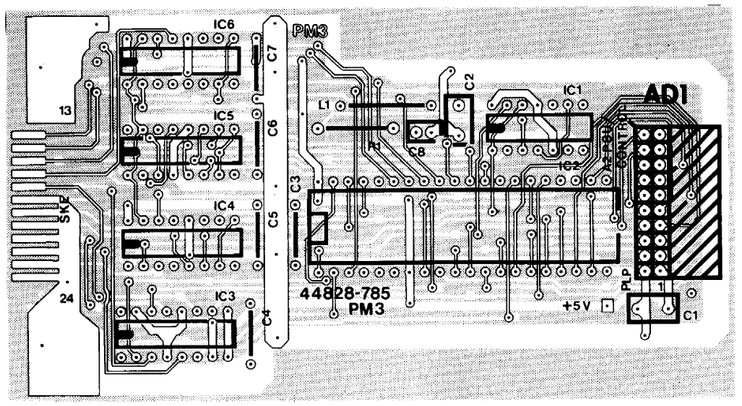
2 PLN 10 POS SIL KEYWAY POS 6

Attenuator, ACO

Fig. 9

Sep. 86 (Am. 2)





GPIB module, component layout, AD1

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Fig. 10a

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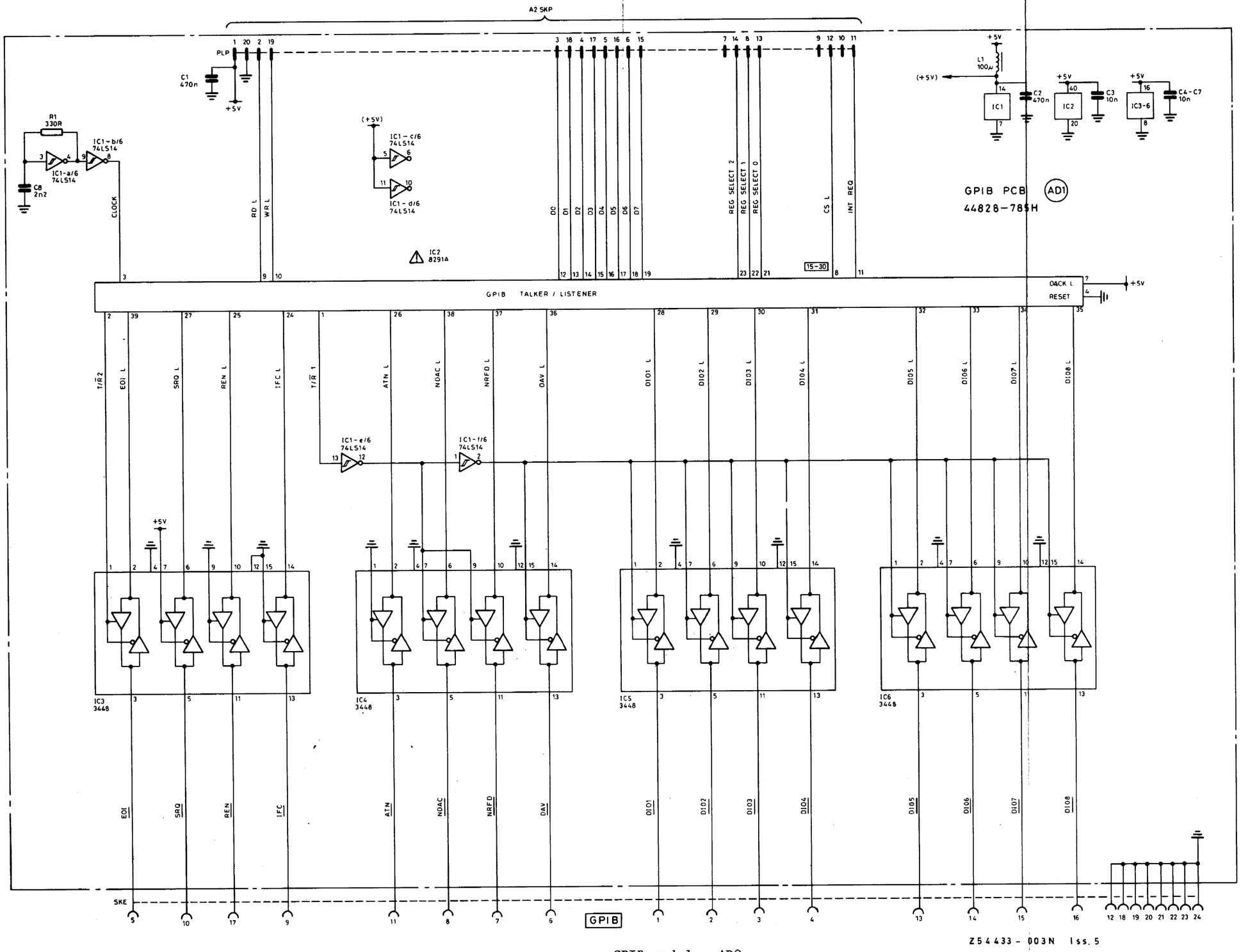

1. COMPONENT MARKED ⚠ IS STATIC SENSITIVE, SEE PCH 22810 FOR PRECAUTIONS.
2. UNDERLINED LABELS REFER TO GPIB TERMS WHICH ARE NEGATIVE TRUE. ALL OTHER LABELS ARE POSITIVE TRUE.
3. PLP: 20 POS. DIL.
4. DIGITS IN BOX ☐ SHOW LATCH ADDRESSES WHEN USING SECOND FUNCTION 3.

GPIB module, ADO